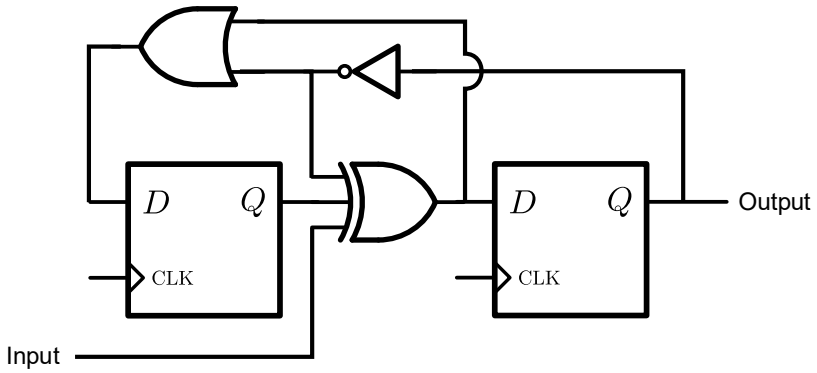
Synchronous Digital System Question

$t_{\text{period}} = 20\ ns, t_{\text{setup}} = 2\ ns$

$t_{\text{XOR}} = t_{\text{OR}} = 5\ ns, t_{\text{NOT}} = 4\ ns$

Input changes 1 ns after clock trigger



A) What is the max t_{C2Q}?

B) If $t_{\text{C2Q}} = 3\ ns$, what is the max t_{hold}?

Walkie Talkie Base Station Design

More SDS practice

For an n-bit ripple-carry adder, what is the shortest and longest time that output S changes after each clock cycle?

- A, B, c_0 from registers (show up at t_{C2Q}); S goes directly to a register input.
- Assume all gates have a delay of 1 ns; use variables for all other timing values