

Exercise 1 –Pulse Generator

a) Draw an FSM diagram for the Pulse Generator.

b) Create the SystemVerilog Implementation of this module

```
Module pulse (input logic clk, reset, in, output logic out);
```

```
endmodule // pulse
```

Exercise 2 – Block Diagrams and Top Modules

a Draw your block diagram for the Psychic tester

b Given these modules, Implement the Top module for psychic tester

```
module genPatt (clk, rst, pattern, next);  
module userIn (clk, rst, guess, submit, {guess_ext, submit_ext});  
module checkGuess (pattern, guess, correct);  
module countRight (clk, rst, correct, submit, next, psychic);  
  
module psychic_tester (clk, rst, guess_ext, submit_ext, psychic);  
    input logic      clk, rst, submit_ext;  
    input logic [3:0] guess_ext;  
    output logic     psychic;
```

```
endmodule // psychic_tester
```

c Implement *DE1_SoC* to connect to hardware

Use SW[3:0] as guess,
~KEY[3] as rst (reset),
~KEY[0] as submit, and
LEDR[0] as psychic.

```
module DE1_SoC (CLOCK_50, SW, KEY, LEDR);  
    input logic    CLOCK_50;  
    input logic [9:0] SW;  
    input logic [3:0] KEY;  
    output logic [9:0] LEDR;
```

```
endmodule // DE1_SoC
```