Intro to Digital Design
L10: Wrap-up

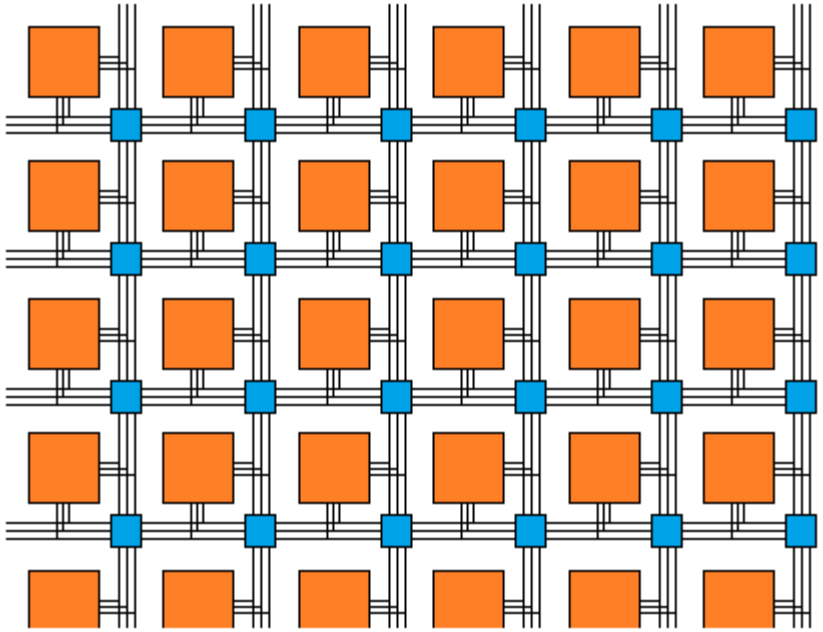
Instructor: Naomi Alterman

Teaching Assistants:

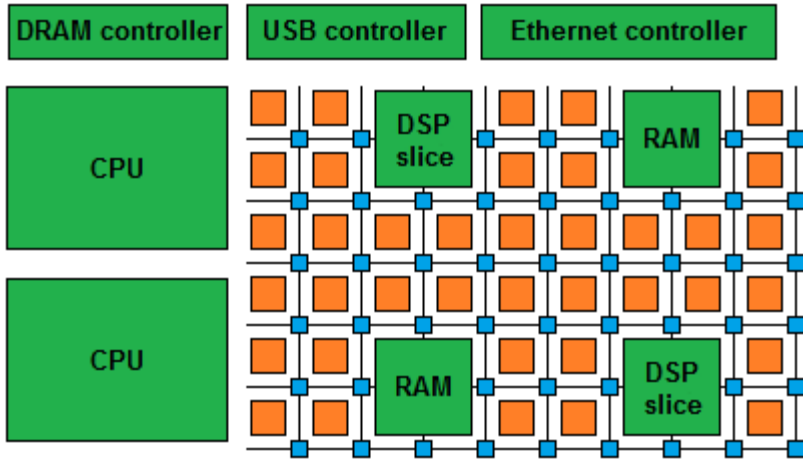
Derek de Leuw
Isabel Froelich
Kevin Hernandez
Aarjav Jain
Packard Stephenson

The "SoC" in "DE1-SoC"

- "System on a Chip"

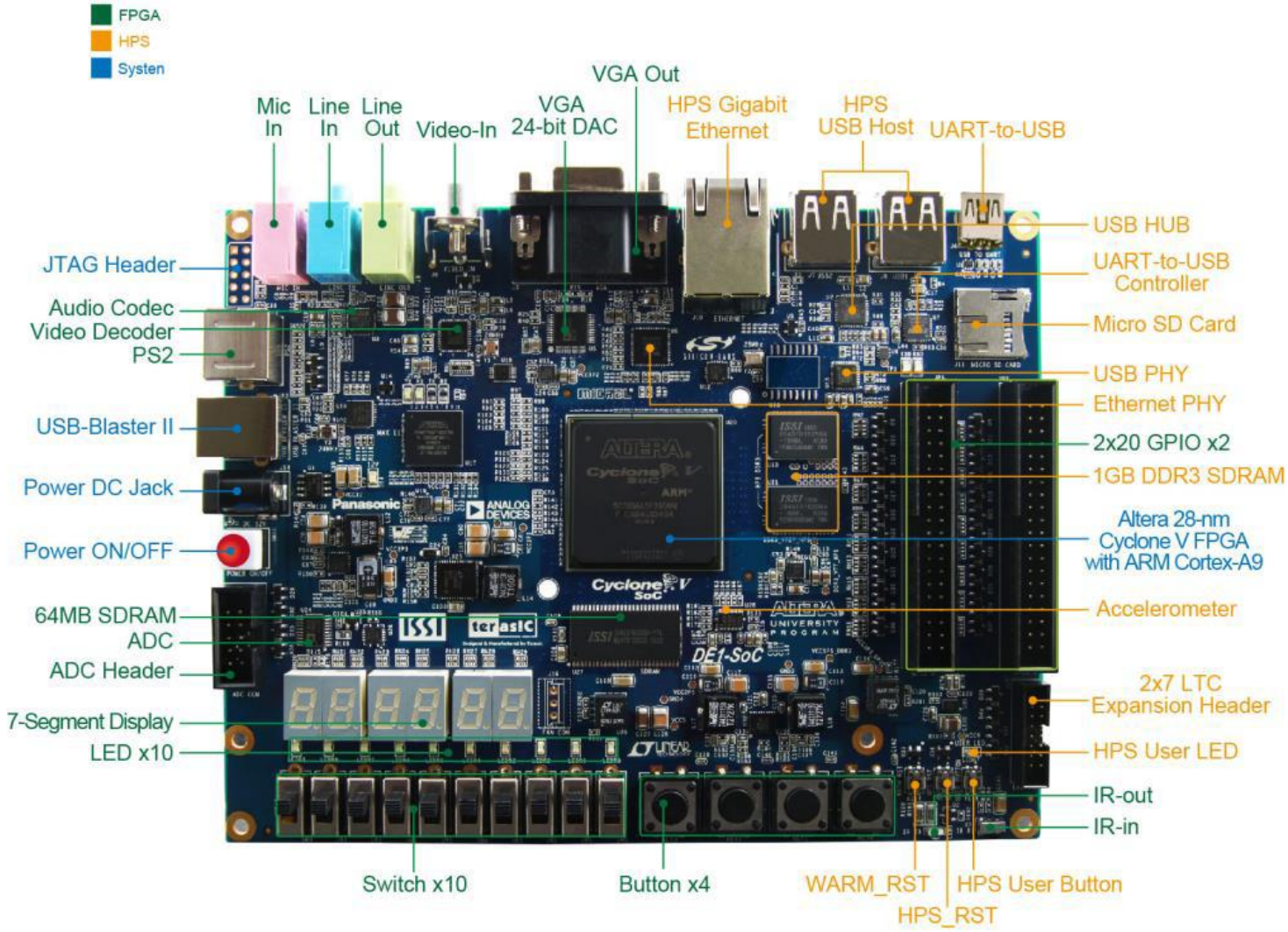


"Clean slate" FPGA: programmable gates and routers

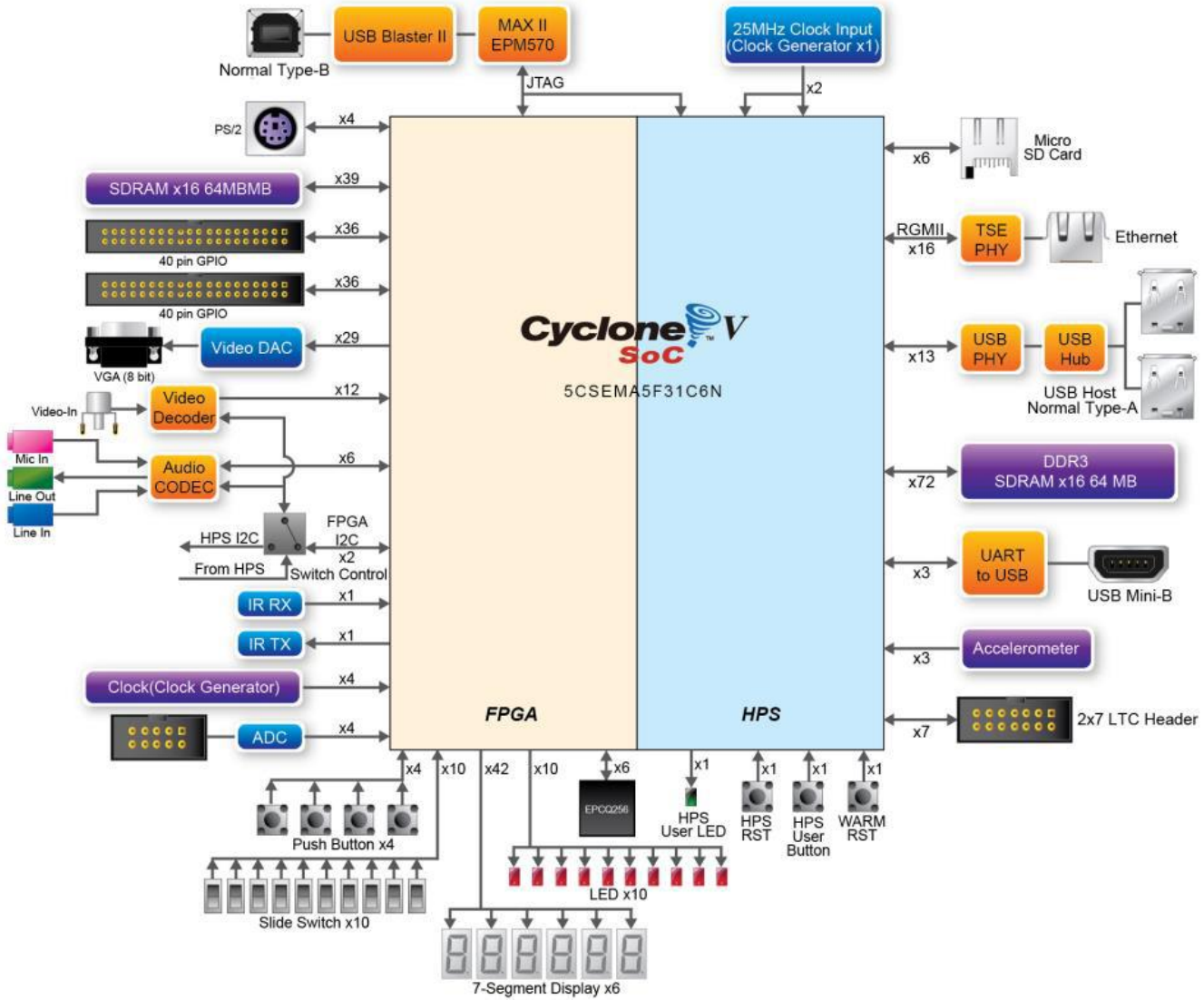


Modern FPGA: lots of hard, not-field-programmable gates

DE1-SoC Board



DE1-SoC Board



FPGAs vs. CPUs

- Individual CPUs designed to handle sequential instruction execution
  - Design and layout determined by architecture
  - Computations "limited" to instruction set
  - Powerful, but also requires things like OS

- FPGAs
  - Programmable, so specially-designed logic for application
    - But can be difficult to specify certain applications
  - Good for parallelizing computations
    - Can perform separate computations if separated via routing

Course Wrap-Up

- Combinational Logic
  - Karnaugh Maps
- Sequential Logic
  - Timing Considerations
- Finite State Machines
- Routing Elements
  - Multiplexor, Encoder, Decoder, Demultiplexor
- Computational Building Blocks
  - Adders, Registers, Shift Registers, Counters
- *SystemVerilog*

New Best Friends

- Multiplexors
  - Logic – can implement arbitrary logic as LUTs
  - Routing – select between many simultaneous computations

- Flip-flops
  - Store information
    - registers, shift registers, counters, FSMs, RAM cells
  - Synchronization of system
    - "Holds up" signals so feedback loops only iterate once per clock cycle
  - Filter out circuit hazards and glitches
  - Gotta watch out for metastability

Takeaways

- Hardware design is all about computation in space rather than computation in time
- Modern EDA tools and design methods let us do a lot without needing to know much about actual circuitry
  - Verilog is a "high level" way to produce the "lowest level" of computing components!
  - Sufficient level of abstraction for many cases
- … but it's a leaky abstraction, and the hardware details are important
  - Timing especially – synchronization, metastability
  - Design affects speed, power, size

Takeaways

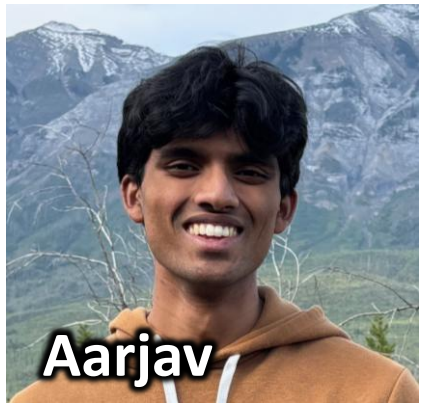
- You now know how to design and implement complex digital circuits!
  - DE1-SoC ($377): http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&No=836

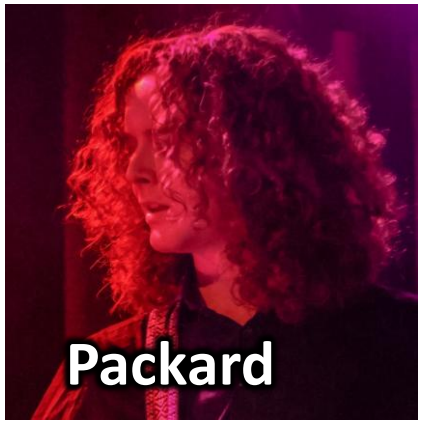
- Future classes
  - EE 205/215 – details of electronics
  - EE/CSE 371 – digital design techniques and considerations (algorithms, communication, complexity)
  - EE/CSE 469 – computer architecture (CPU design)

Final Words

- Thank you for letting me share some of my favorite things in the world with you this quarter, it's been a privilege 🙏

- Let's give a round of applause to the **dream team**!





Course evals

- Due this **Sunday 6/7**
- Two anonymous forms:
  - An official course evaluation
  - TA evaluation form (fill out once per TA)

- Links to both forms:

  https://courses.cs.washington.edu/courses/cse369/26sp/evals.html