Field Programmable Gate Arrays (FPGAs)

- Readings: B.6-B.6.5

Logic cells imbedded in a general routing structure

Logic cells usually contain:

- 6-input Boolean function calculator
- Flip-flop (1-bit memory)

All features electronically (re)programmable
Using an FPGA

Verilog

FPGA CAD Tools

Bitstream

Simulation
FPGA Programming

![Diagram of an FPGA's 4:1 MUX with bitstream data]

○ = 1 memory cell (stores 1 bit of info)
FPGA Combinational Logic

How can we use Muxes and Programming bits to compute combinational binary function $F(A,B,C)$?

- Creates a “LUT” or lookup table.
FPGA Sequential Logic

- How do we put DFF’s onto LUT outputs only when we need them?

- Creates a “LE” or logic block
How do we combine LE’s to build larger functions?

This is an Altera “LAB”.
FPGA Global Routing

- Can’t do all-to-all/crossbar routing, so what?

```
  LAB
  ┌──┐  ┌──┐
  │  │  │  │
  │  │  │  │
  └──┘  └──┘

  LAB
  ┌──┐  ┌──┐
  │  │  │  │
  │  │  │  │
  └──┘  └──┘
```
FPGA CAD

- CAD = “Computer-Aided Design”

Verilog

- Tech Mapping: Convert Verilog to LUTs
- Placement: Assign LUTs to specific locations
- Routing: Wire inputs to outputs
- Bitstream Generation: Convert mapping to bits