# CSE352 Autumn 2014 Homework \#4 

Due In Class Friday 10/31/2014

Please write your name and student ID at the top right corner of each page, and staple or paperclip your work together. We are NOT responsible for losing papers that were not stapled or paperclipped together.

Complete the following questions. Please write legibly and try to draw clean diagrams. Spaghetti wiring in circuit diagrams is difficult to grade. We will not grade work that is too heavily encrypted for us to read (i.e. we can't read it, we can't grade it). Please consider typesetting your work if you think that it may not be legible to the grader. This is an individual assignment. You may not work in groups. Justice will be enforced if you are caught cheating.

## Problem 1 Carry Select Adders

This question is about Carry Select Adders, another type of adder that is faster than the straightforward ripple carry adder. In the Carry Select Adder, the bits are broken into blocks. The computations within each block are performed simultaneously, giving a speed up due to parallelization. Because the carry value from earlier blocks is not initially known in later blocks, each block computes the sum for both possible values of its "carry in" bit. Once a block's true carry in value is known, multiplexers are used to select the correct sum bits (multiplexers on the bottom) and carry bits (multiplexers on the left side).

Ben Bitdiddle and Alyssa P. Hacker are arguing (again) about the best way to implement an 18 -bit carry select adder. Assuming full adders and multiplexers incur the same delay of $n$ Ben argues that the fastest implementation would be to use 3 groups of 6 adders and incur a delay of 8 n as shown below:


Alyssa obviously disagrees and thinks that there is an implementation that has a delay of 7 n . Does such an implementation exist? If so show how it can be done.

## Problem 2 Blast from the Past (Review)

Draw the CMOS transistor implementation of the following Boolean expressions.
Minimize the number of transistors used:
(a) $\overline{(A+B)(D C+E C)}$
(b) $\bar{A} \bar{B}+\bar{C}+\bar{D}$

