Introduction to Active-HDL

TUTORIAL #0:
INTRODUCTION TO CREATING AND SIMULATING SIMPLE SCHEMATICS

This tutorial will introduce the tools and techniques necessary to design a basic schematic. The goal of this tutorial is to familiarize you with Active-HDL and to help you complete your assignment. After finishing this tutorial you will know how to:

- Start Active-HDL.
- Create a new workspace and design
- Add and remove files to and from a design.
- Place parts in a schematic design from the built-in library.
- Use wires in a schematic design.
- Run a basic simulation.

Start Active-HDL

First, start Active-HDL by double-clicking the icon located on your desktop. If the icon is not present then go to Start and select "Active-HDL 7.3" under the Programs menu.

Create a new workspace

A workspace holds your designs, and each design may consist of many files (i.e. schematics, Verilog source code, etc). When you open Active-HDL, you will be presented with the Getting Started window. Once you have created other workspaces, they will appear in the field at the center of the Getting Started window. The "More…" button allows you to browse for existing workspaces.

1. Select the "Create new workspace" option. This opens the New Workspace window:

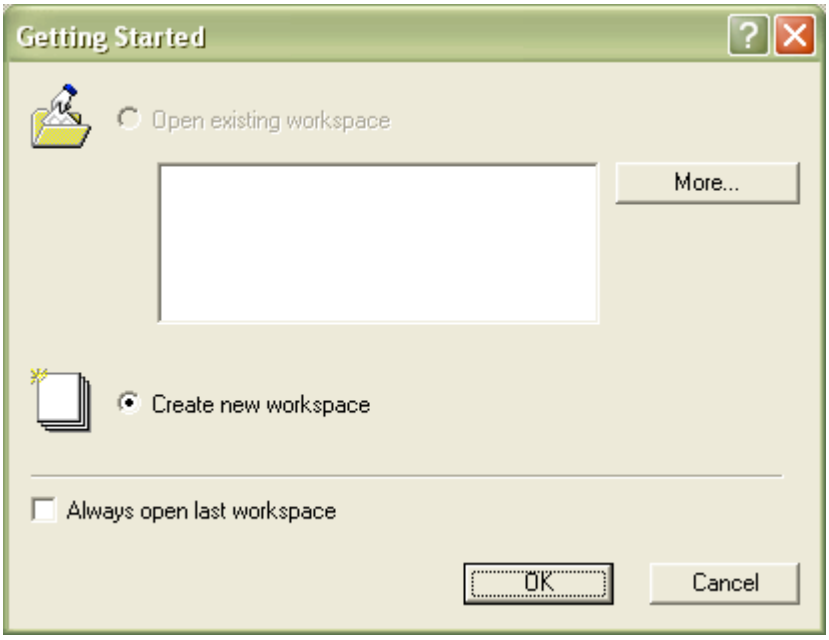


Figure 1

2. Enter a **descriptive** name into the "Type the workspace name field.

3. Change the workspace directory by entering it in the "Select the location of the workspace folder" field, or use the "Browse" button to select the new directory. We strongly recommend you use your student drive. Note: Files saved to the local drive will be automatically deleted on logout.
4. Select the "Add New Design to Workspace" check box if it is not already checked.
5. Your New Workspace window should look like Figure 2. If so, click the OK button, and continue.

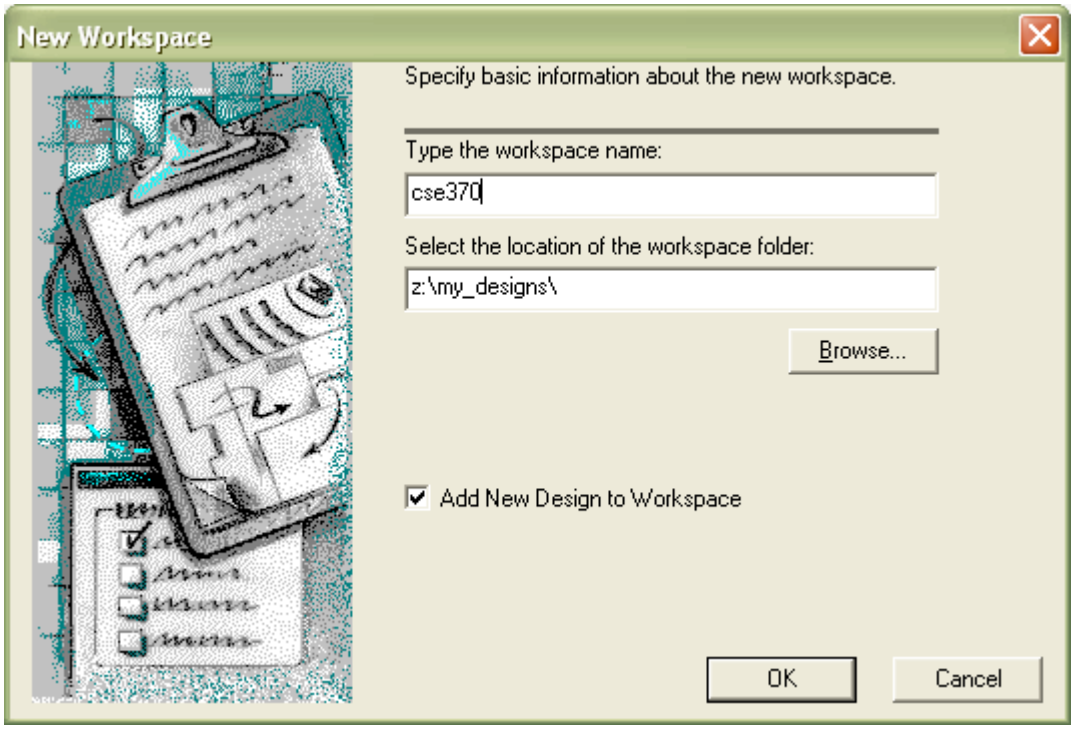


Figure 2

Create a design

After creating a workspace, the New Design Wizard walks you through creating a design. A design can consist of one or more Verilog modules, schematics, and other design files. A workspace, as mentioned earlier, can contain one or more designs. You can add more designs later by selecting File/New/Design in the menu bar. For now, we will add the first design to the workspace by following the steps provided on the following pages.

1. Click the "Create an Empty Design with Design Flow" radio button. Then click the Next button.

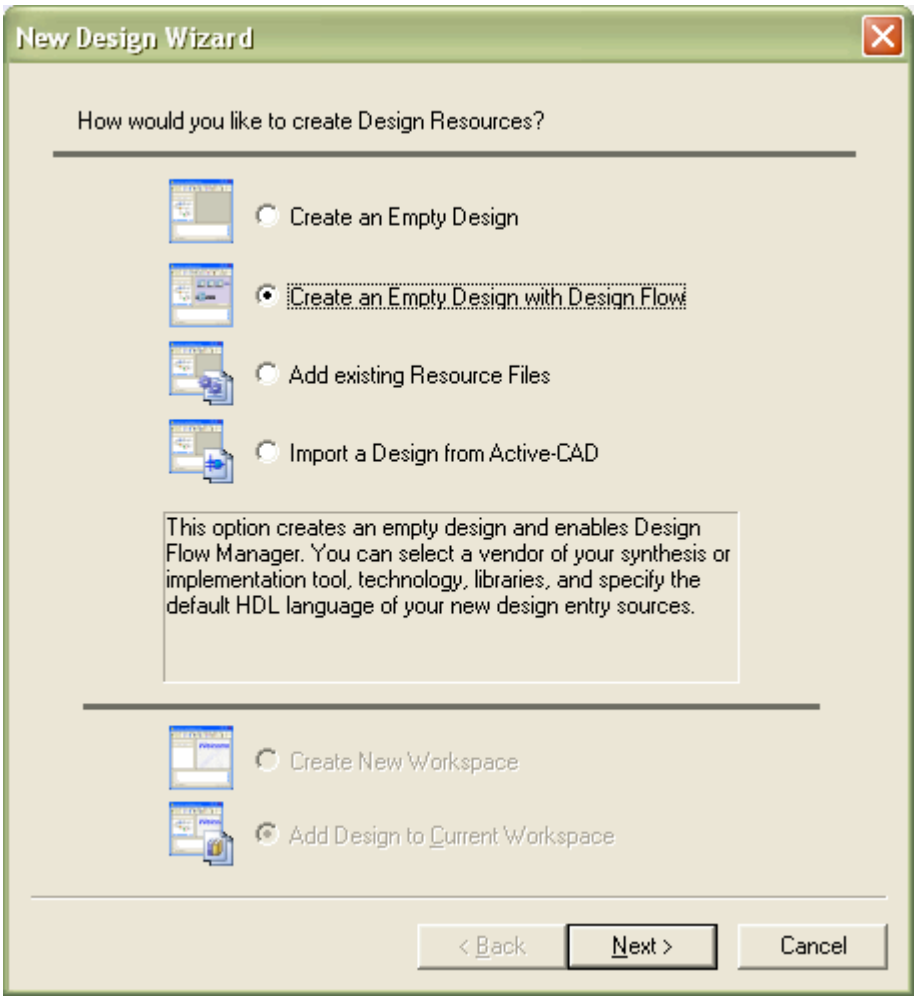


Figure 3

2. Find the "`Block Diagram Configuration`" field and select the "Default HDL Language" option. Make sure the "`Default HDL Language`" field is set to "VERILOG." Your New Design Wizard window should look like Figure 4. If so, then click the Next button.

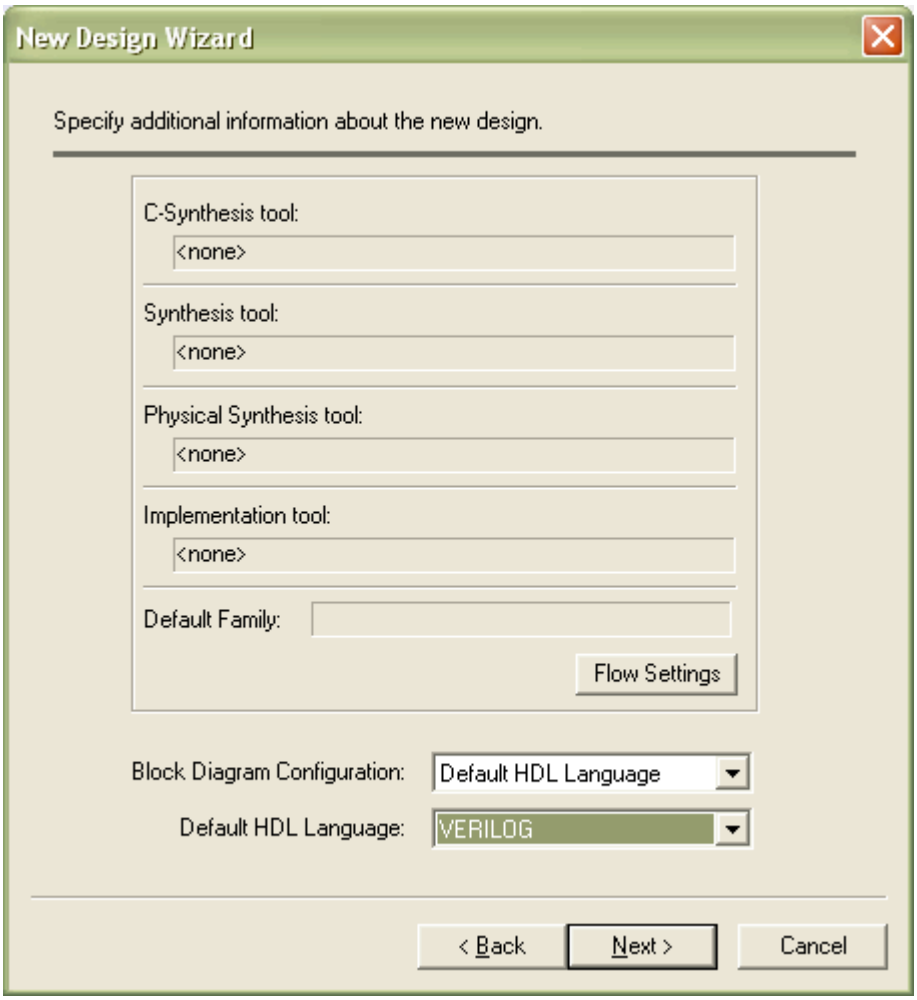


Figure 4

3. In the "Type the design name" field, type a name for your new design. **The name must contain only letters, numbers, and underscores ("_"), and cannot start with a number (i.e. 4bitadder is invalid, however four_bit_adder is valid).** Use **descriptive** names that do not match file names, other design names, or workspace names. By default, the design directory is under the workspace directory, and the name of the default working library of the design is the same as the design name. Leave these default values alone. **Warning: the directory path should <u>not</u> contain any spaces in it.** Your window should look like Figure 5 with a more descriptive name than "combo_logic".

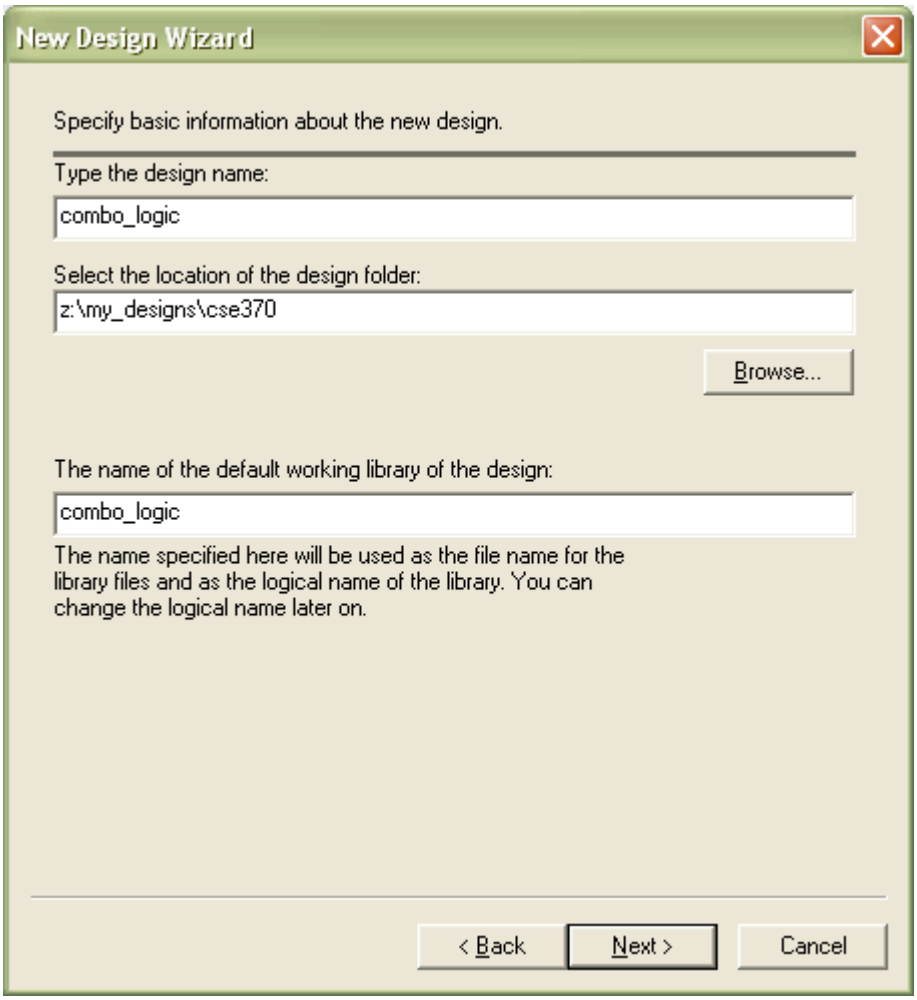


Figure 5

4. Double check your file name and location, then click the Next button.
5. Make sure that your design name is correct and the design directory is correct in the window that follows (not shown). If not, click the Back button to make any changes, or click the Finish button to create the design.

Add a Block Diagram (schematic) file

At this point your screen should look like Figure 6. The frame on the left is called the Design Browser and lists all of the components in your design. The frame on the bottom is the Console and is where status and error messages are printed. If these frames are not open, or if you have closed them by accident, you can open them by going to View in the menu bar. In the center of the screen is the main window where you will draw your schematics. When your design is first opened, the Design Flow Manager opens in this window. We won't be using this tool during this tutorial. At the top of this window is the Standard toolbar. Finally, notice the tab at the bottom left side of the main window. As you create schematics and other components in your design, you can use the tabs at the bottom of this window to make the corresponding file active in the main window.

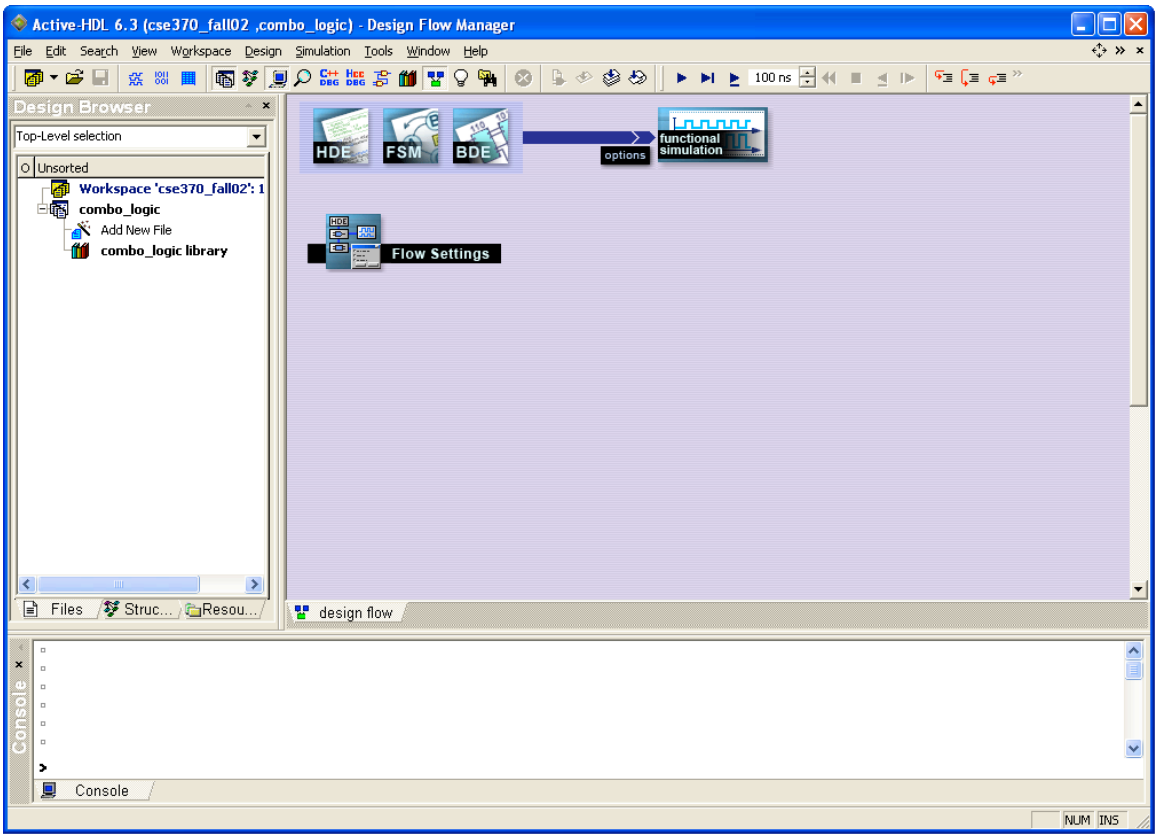


Figure 6

1. Double-click the “Add New File” option in the Design Browser (Figure 7). This will open the Add New File window.

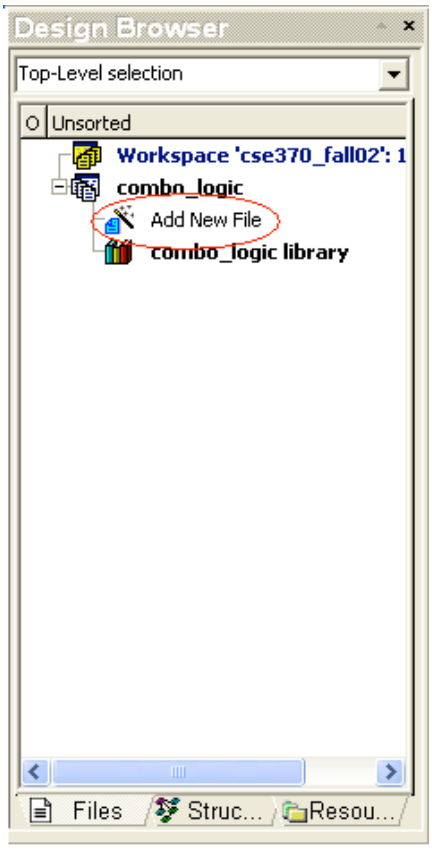


Figure 7

2. Click the Empty Files tab in the Add New File window. Select the Block Diagram icon, type in a descriptive name, and then click the OK button (Figure 8).

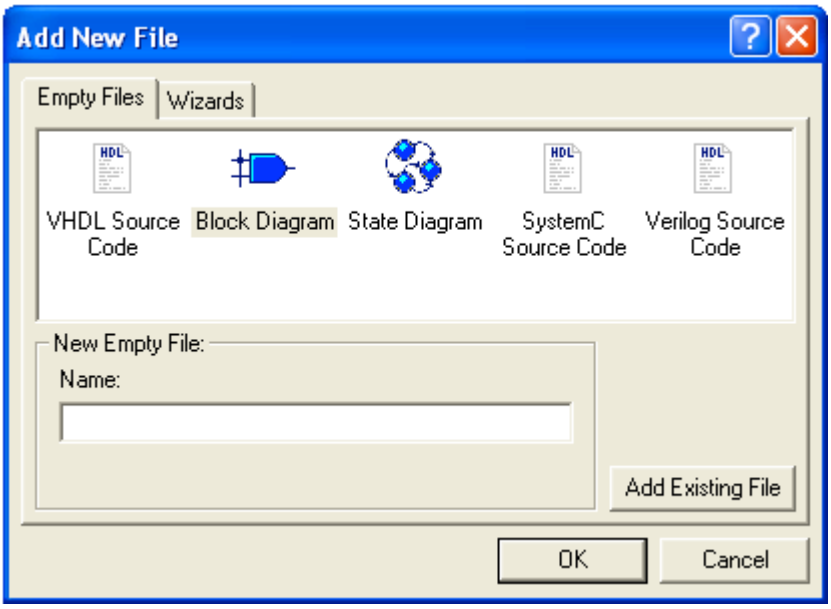


Figure 8

3. Notice this schematic file has been added to the design in the Design Browser on the left. Schematic files in Active-HDL are called Block Diagram files and have an extension of ".bde". The question mark means the file has not been compiled yet, which we will get to later. Also, new toolbars have been added below the standard tool bar, which are used to edit block diagrams.

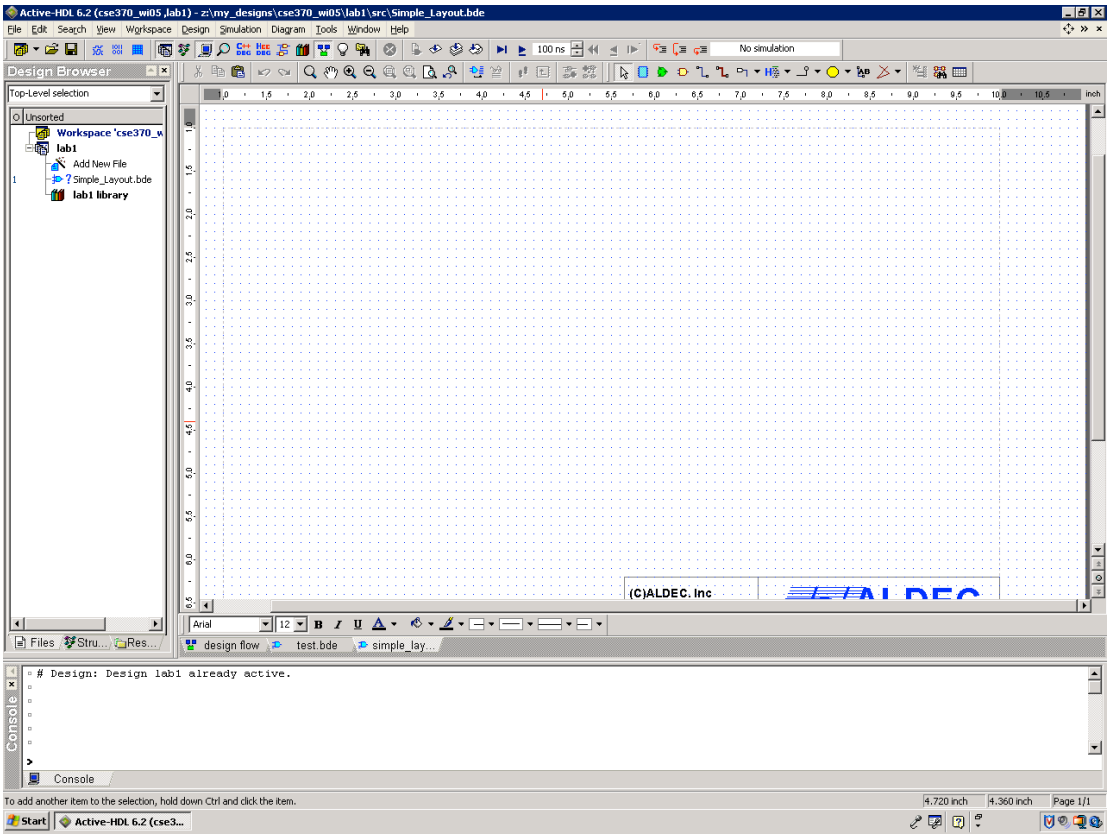


Figure 9

Place parts into your schematic design

Now you are ready to build your gate logic. The steps below will teach you how to add basic gates to your schematic and how to add single bit input and output terminals. (**Note**: this tutorial uses the icons in the toolbars and other shortcuts to access most of the tools in Active-HDL; however, all the commands accessed from the toolbars can be found in the menu as well). Additionally, you will need to know how to move and delete gates to clean up your design's appearance.

Figure 10 is the final version of the schematic you will be drawing. Your final design should look similar with two inputs (A & B), two gates (AND & OR), and two outputs (Y & Z)*.

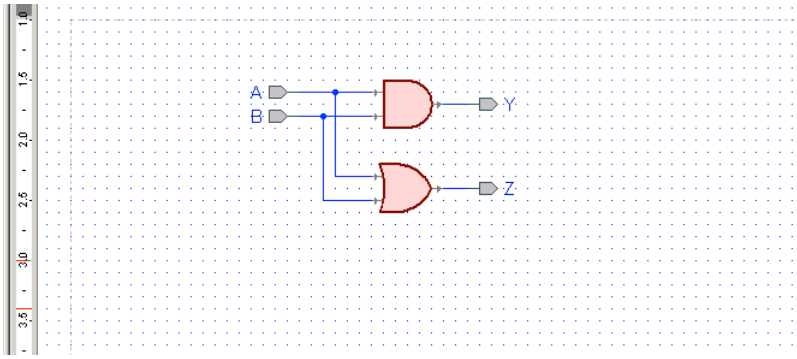


Figure 10

*Some of the components you use may differ in appearance from the components shown in this tutorial.

1. You are required to use the components located in the standard class library called "lib370". **Do not use built-in symbols**. Therefore, you need to add the symbols for the components in the standard class library to the symbols toolbox using the Library Manager. Open the Library Manager by clicking the Library Manger icon in the toolbar.

Figure 11

2. Locate the lib370 library in the left frame of the main window, and right click it (Figure 12).
3. Select the "Add to Symbols Toolbox" option.

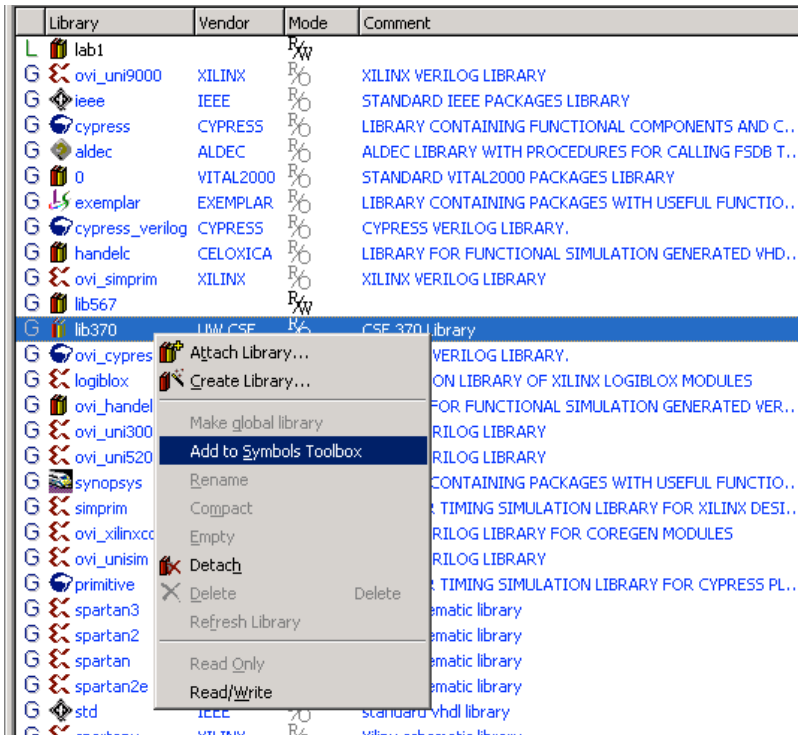


Figure 12

4. Close the Library Manger by clicking its icon in the toolbar, or select File/Close.
5. Open the Symbols Toolbox by clicking the Symbols Toolbox icon in the toolbar (Figure 13).

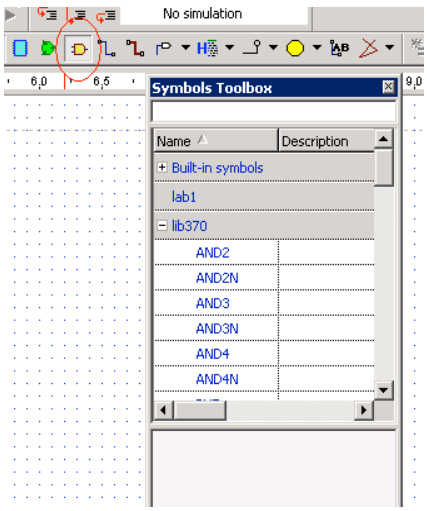


Figure 13

6. Click the plus symbol to the left of the “lib370” option to expand the list. Scroll down the to find the desired part from the list, or type in the name of the part in the field at the top of the Symbols Toolbox to search the list.
7. Click on the parts name in the list and notice that its symbol appears at the bottom of the Symbols Toolbox.
8. Add the part to your schematic by dragging the symbol from the Symbols Toolbox into your design.

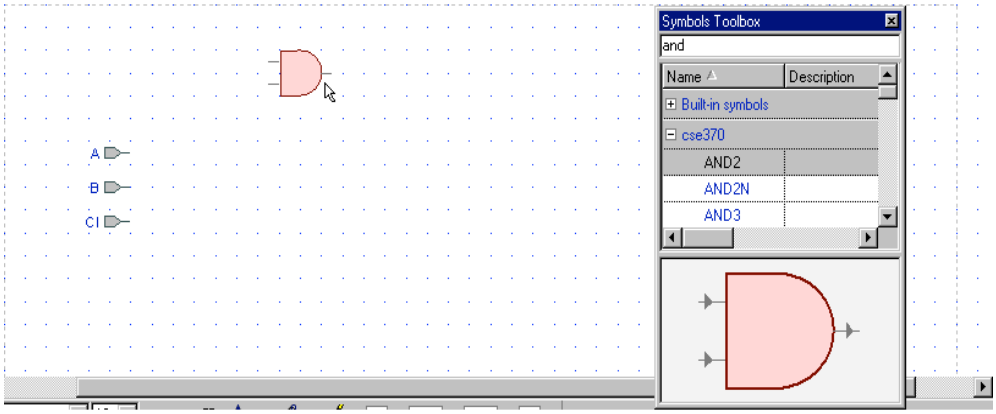


Figure 14

9. Active-HDL uses the standard Windows user-interface to select, move, and copy items in the schematic (i.e. drag, Ctrl-drag for copying multiple parts, Ctrl-z for undo, etc.). Figure 15 is an example of Ctrl-drag.

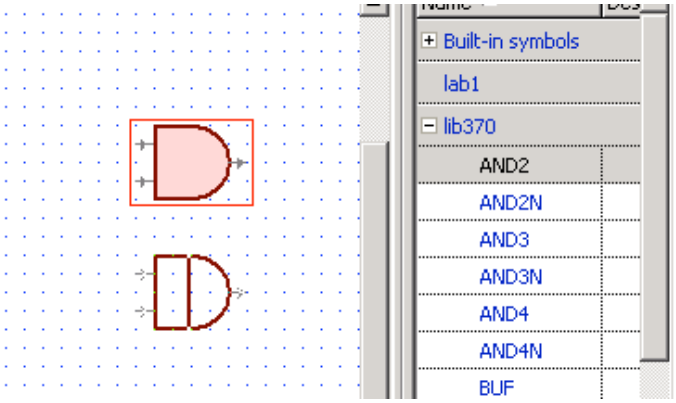


Figure 15

10. To add a terminal click the drop down arrow next to the Terminal icon in the toolbar (or click Diagram/Terminal in the menu bar). Click the “Input” or “Output” option in the expansion menu.

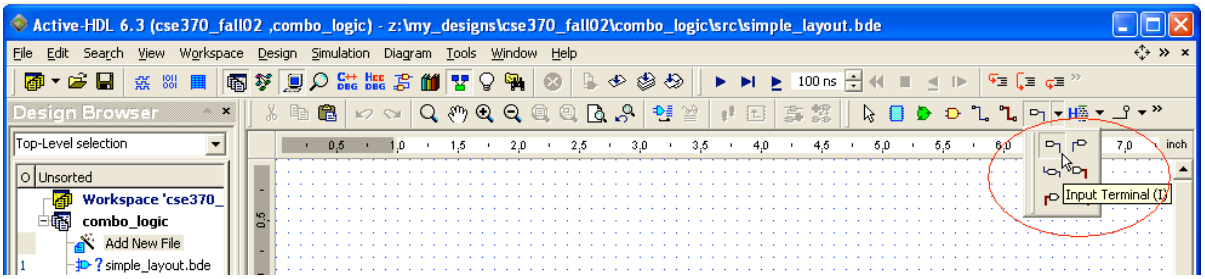


Figure 16

11. Click in the schematic where you want the terminal.
12. Notice that you can continue to click and add multiple terminals. To stop adding terminals, press the Esc key. **Note**: The Esc key is very useful to "get out" of just about any process (i.e. drawing wires, placing components, etc).

Moving gates and terminals is as easy as clicking and dragging the part to the new location. Additionally, the arrow keys are very useful for moving components precisely where you need them in the schematic. To delete parts, simply click the part to be deleted (when properly selected, the part will be outlined in a red box), and then press the Delete key.

Using wires in Active-HDL

This part of the tutorial will show you how to make connections using wires, how to move the wires, how to name wires, and how to delete wires.

1. Click on the Wire icon in the toolbar (see Figure 17).

Figure 17

2. Now click anywhere in the schematic and drag your mouse to the point in the schematic where you want the wire to end. Clicking on a port or terminal will connect an end of the wire to that port or terminal, clicking on another wire will create a junction, clicking on an empty space in the schematic will create an anchor or bend in the wire at that point, and double-clicking an empty space in the schematic will create an end to the wire at that point.
3. When you are done placing wires, go back to select mode by pressing the Esc key or clicking the Select Mode button in the toolbar.

   Removing wires:

   a. Select the wire by clicking on it (the selected wire will turn red).

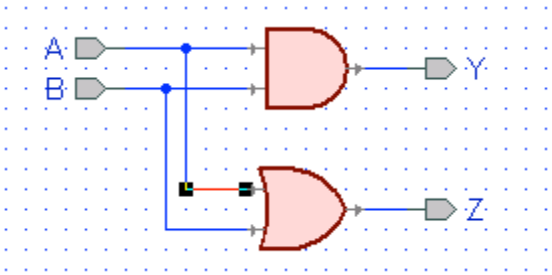


Figure 18

   b. Press the Delete key.

   Moving wires:

   a. Click and drag on the wire or part of the wire to be moved.
   b. Drag your mouse to the new location and release the button.

Checking, saving, and compiling your design

At this point you should have a schematic with gates and terminals connected using wires. However, your file in the Design Browser is still preceded by a question mark. Before you can run simulations you need to compile your design, at which point the question mark will become a green check mark if all is well, or a red "x" if there are errors.

1. Always save your files first. To do this, click the Save icon in the toolbar, or press Ctrl-S with the file's tab active in the main window. Remember to save early and often throughout the design process.
2. Active-HDL provides a "Check Diagram" tool. This tool will verify that the components are connected properly by printing the results into the Design Rule Check report (DRC). Always use the "Check Diagram" tool prior to compiling by clicking the Diagram/Check Diagram option in the menu bar (see Figure 19).

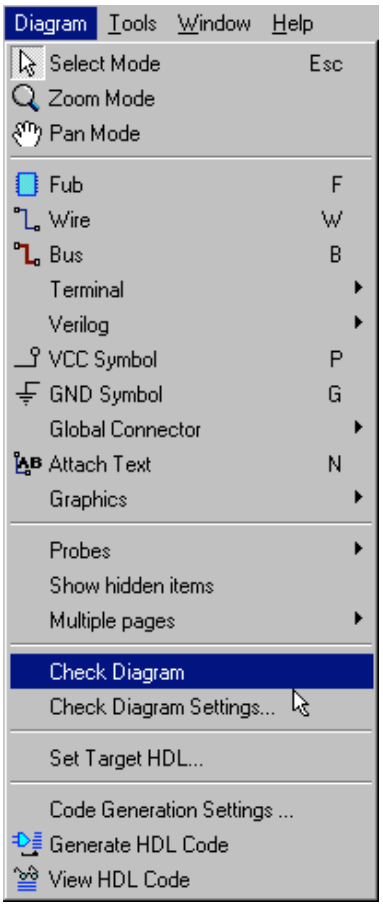


Figure 19

3. When you run the check diagram tool, a DRC report file is created. Open this file by going to the DRC line in the Console and double-click the appropriate line (see 20). This file will list any errors or warnings your design might contain, such as unconnected ports, mislabeled wires and/or terminals, and other connection related errors/warnings. Each error/warning in the report is a hyperlink that will take you to the problematic component in your design. Figure 20 shows an example of a DRC report file for a schematic with an error and some warnings.

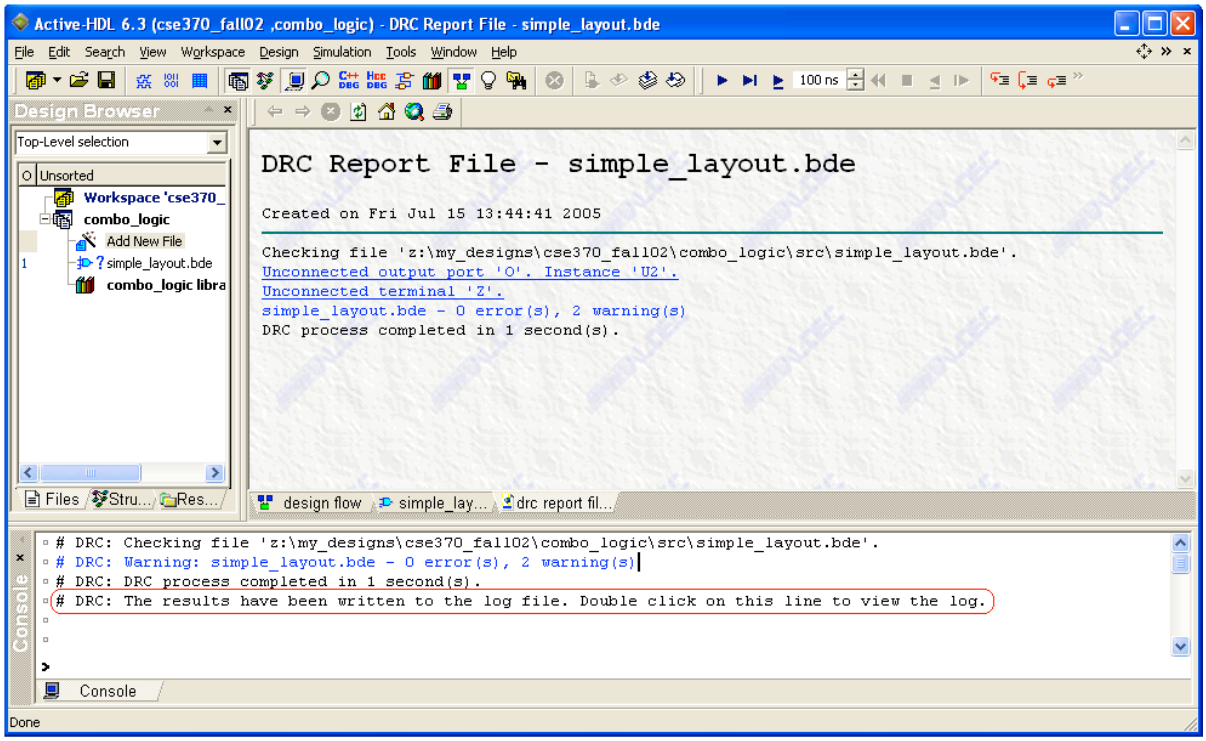


Figure 20

4. After you have checked your diagram and resolved any errors or warnings, click the Compile icon in the Standard toolbar (see Figure 21). The Console window will display the results of the compilation. When compiling a schematic, the console will generally compile successfully even if there are gates and/or terminals that are not connected (in some cases, warnings will be issued for unconnected ports). Therefore, just because a schematic compiles does not mean that it will do what you intended it to do during simulations. This is the reason you need to check your diagram prior to compiling. Figure 21 shows a successful compilation.

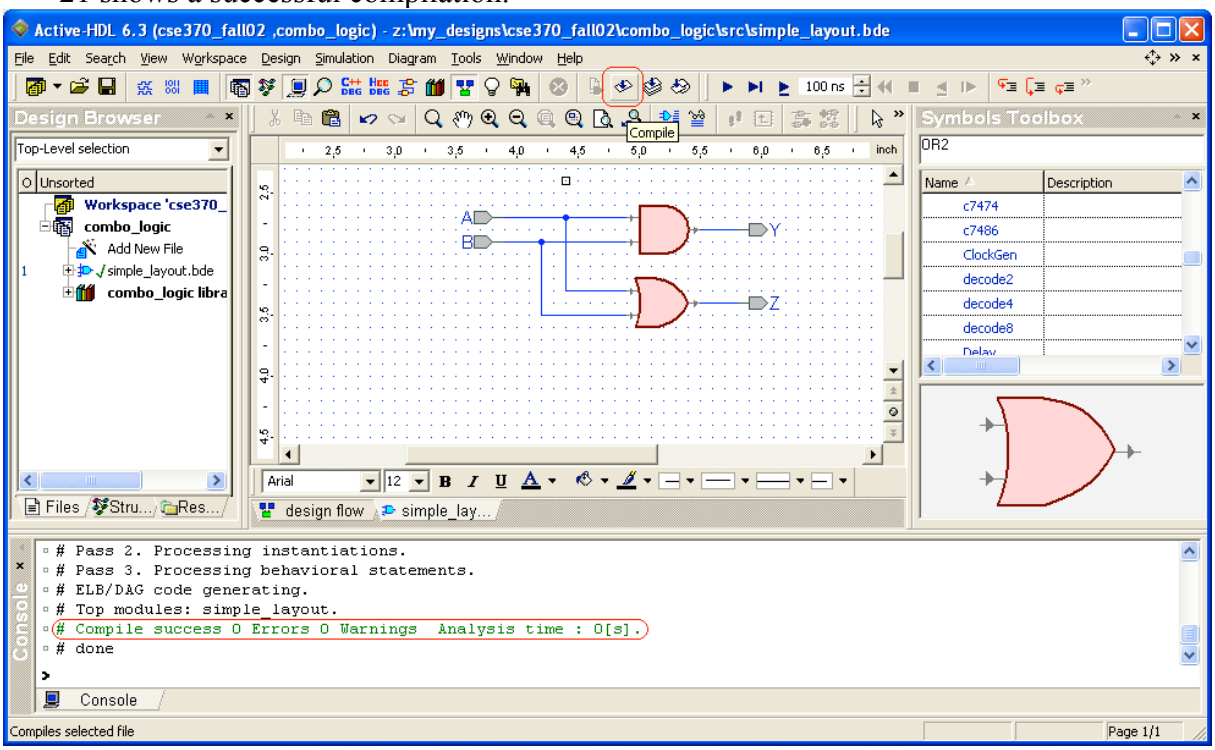
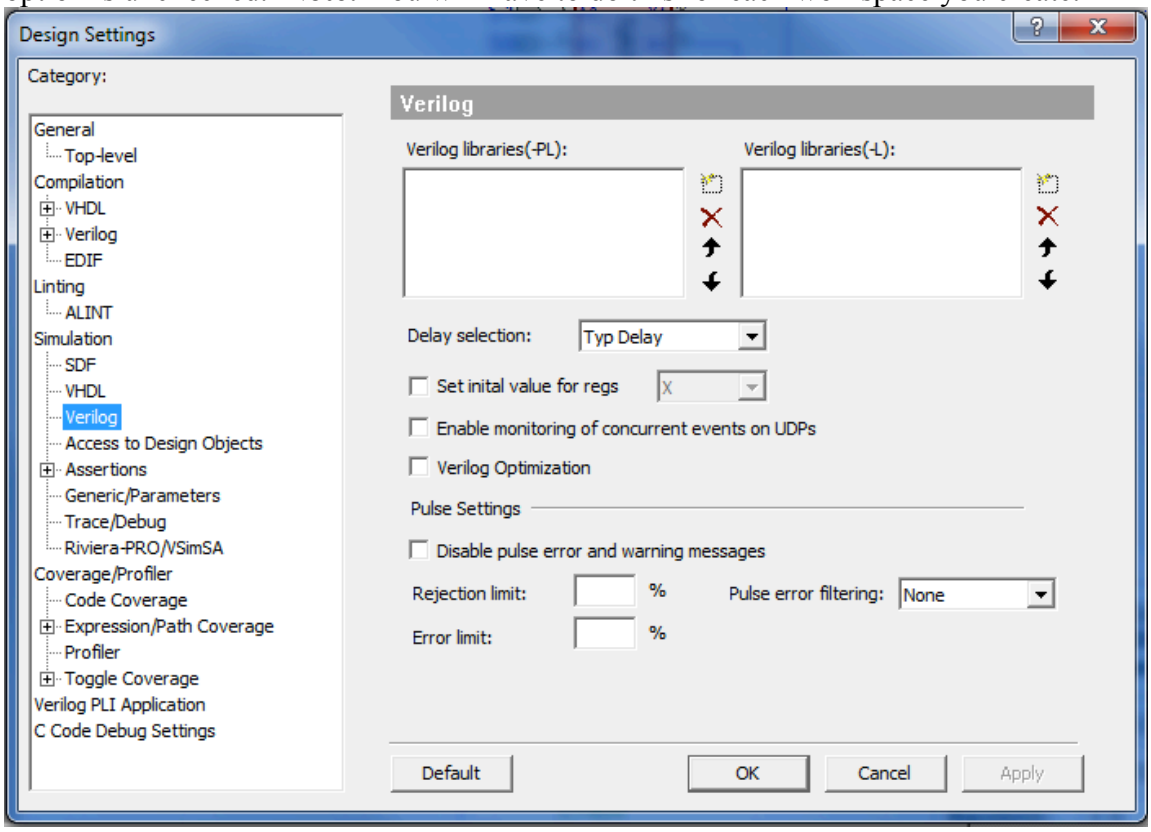


Figure 21

Simulating a design

To ensure that your design functions as you intend, you need to simulate it. This portion of the tutorial will show you how to set the top-level, how to open a waveform, how to add signals to a waveform, and how to use "stimulators". **Important**: close all open waveforms from previous simulations, if any, prior to running a new simulation.

1. By default, Active-HDL comes with Verilog optimization enabled. The details are not important, but our library won't work with the Verilog optimization. Before simulating a design, you will have to disable the Verilog optimization. Open the Design toolbar menu, and click the Settings item. In the window that pops up, look to the left and click the "Verilog" heading, under "Simulation". Make sure that the "Verilog Optimization" option is unchecked. **Note:** You will have to do this for each workspace you create.



2. Before you can simulate a design, you must set the top-level. Since designs can be composed of multiple files or layers, we need to tell Active-HDL which file is our top-level. After you compiled your block diagram file, two files were created: a Verilog file, and a module. Expand your block diagram file list by clicking the plus symbol next to the file name in the Design browser. Continue to expand the list until you see the module, which is proceeded by an "M" icon. **Note**: the following design entities are valid choices when setting the top-level: a configuration ["C" icon], a module ["M" icon], or an EDIF cell ["D" icon].
3. Right click the module.
4. Select the "Set as Top-Level" option. If you do not set the top-level, Active-HDL will "ask" you to do so when you attempt to initialize a simulation.

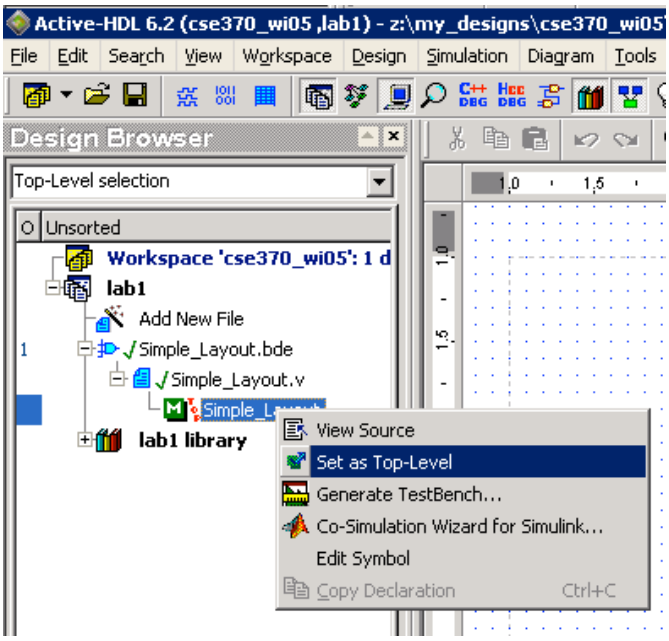


Figure 22

5. Select “Initialize Simulation” under Simulation in the menu bar.

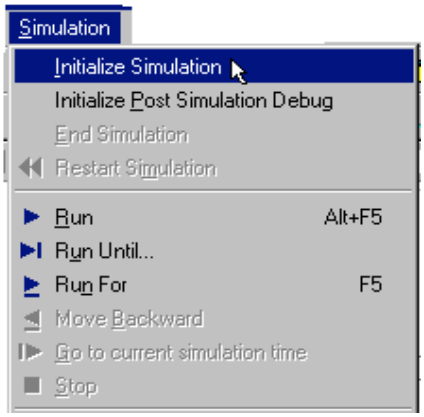


Figure 23

After selecting “Initialize Simulation”, notice in Figure 24 that the Structures tab is opened in the Design Browser.

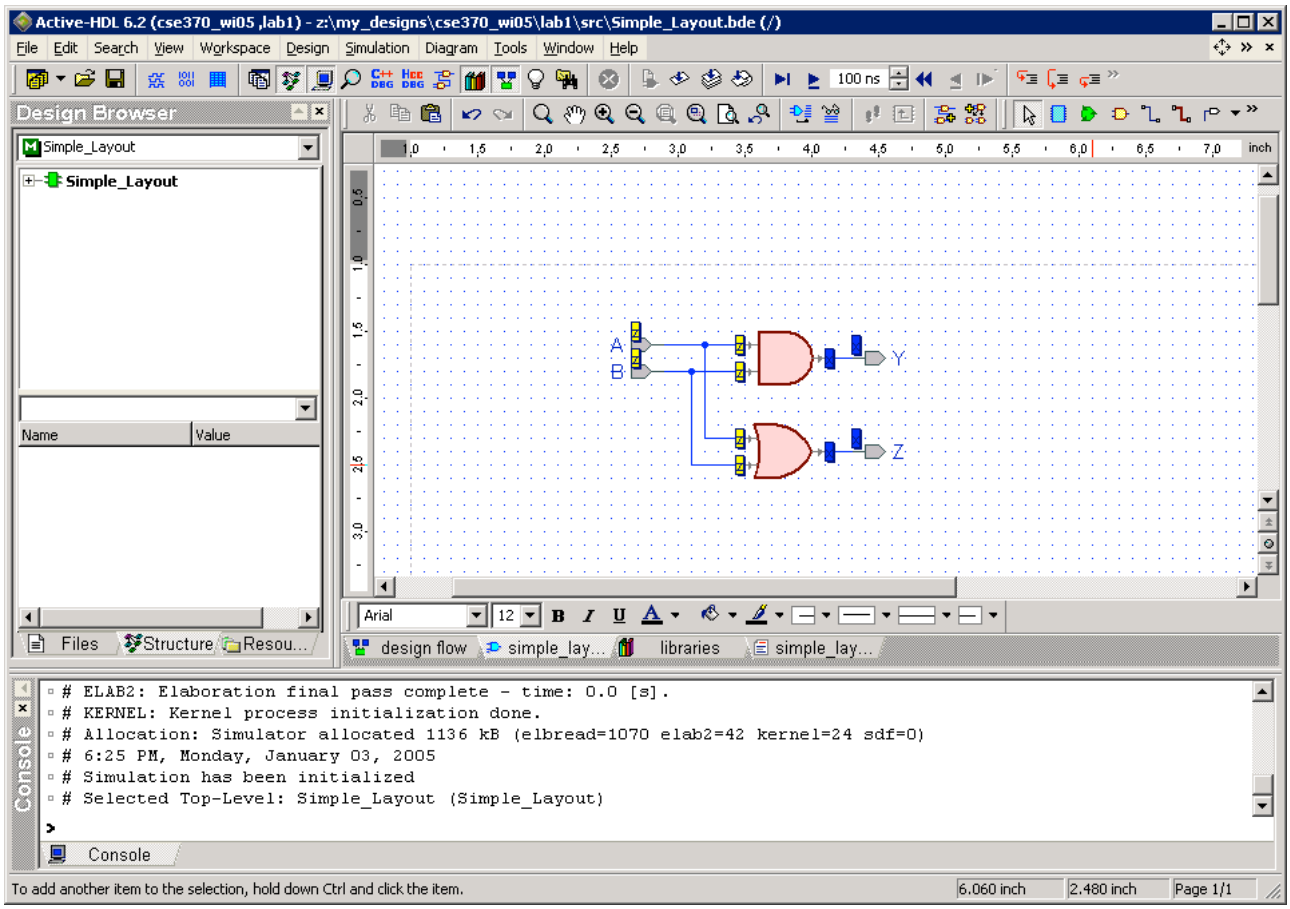


Figure 24

6. Click the New Waveform icon in the Standard toolbar.

Figure 25

7. Click the file name in the top window in the Design Browser under the Structures tab. Notice in Figure 26 how the signals and wires (Nets) appear in the bottom window of the Design Browser.

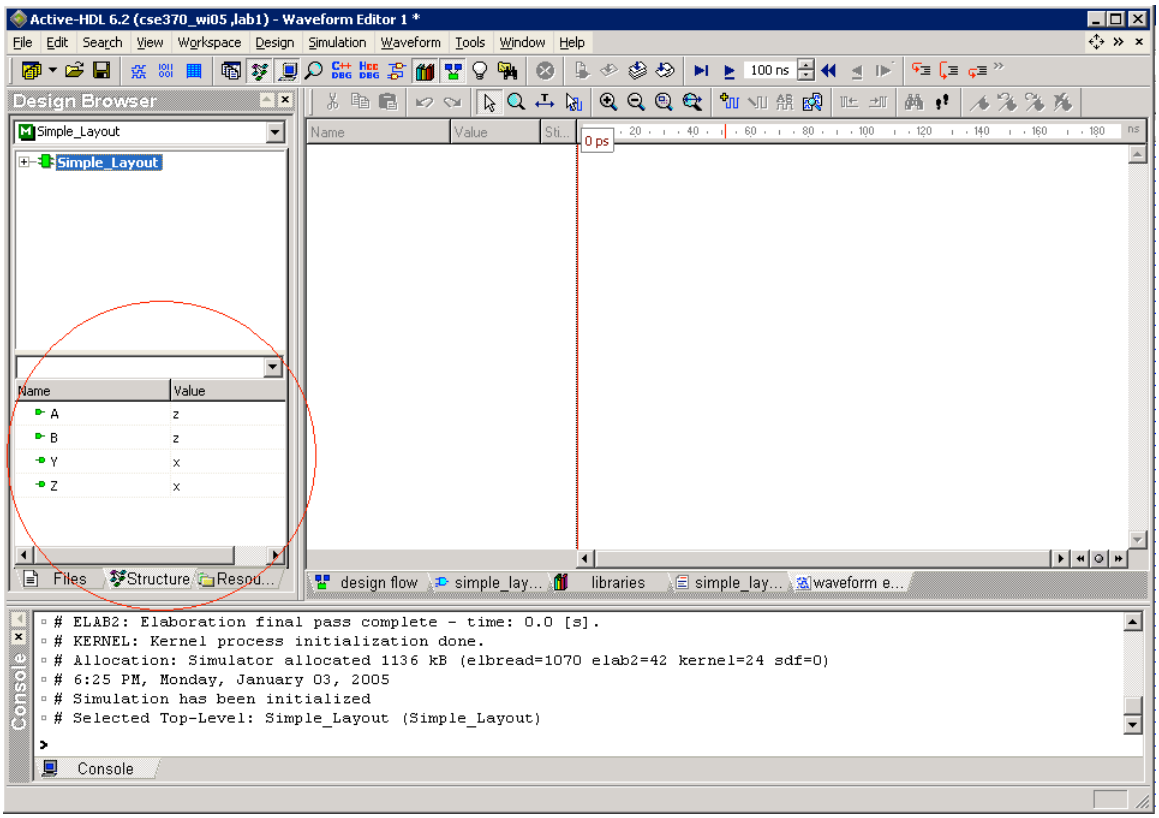


Figure 26

8. Add the signals to the waveform by dragging the signals one by one into the left side of the waveform. A faster method of adding signals to the waveform is to select the signals using the Shift or Ctrl keys. Now you may drag them as described above into the waveform. You can also right-click on a selected signal, and click the Add to waveform option in the pop-up menu as shown in Figure 27.

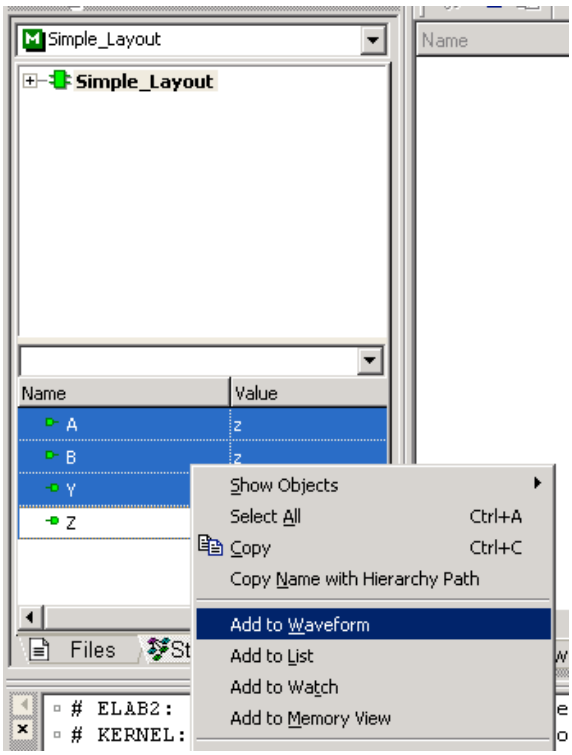


Figure 27

9. To simulate a design, we have to provide values for the input signals. Active-HDL provides Stimulators to drive input signals in a waveform. In the left half of the waveform window, right click on the input signal you wish to stimulate.

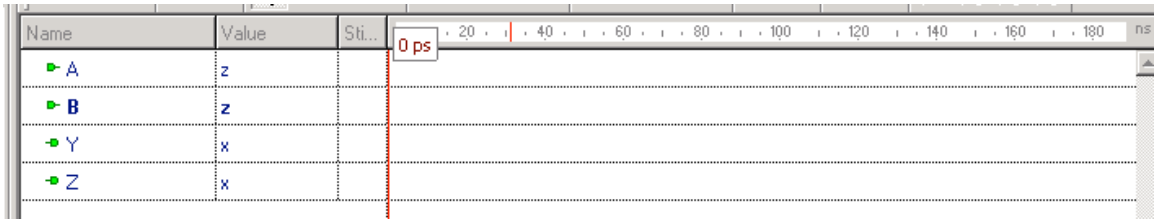


Figure 28

10. Right Click over the name of the signal on the waveform and select the "Stimulators" option in the pop-up menu.

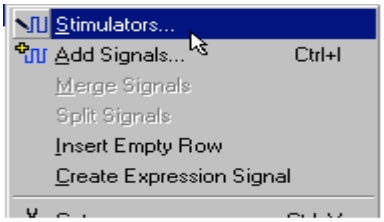


Figure 29

11. The Stimulators window will pop up with the Signals tab active. The large arrow points to a list of stimulators, and your signal is shown on the left side of the window in the signals field. The "Type" list shows the different stimulator options: choose the "Clock" option. See "Using Stimulators" at the end of this tutorial to learn about some of the other options.

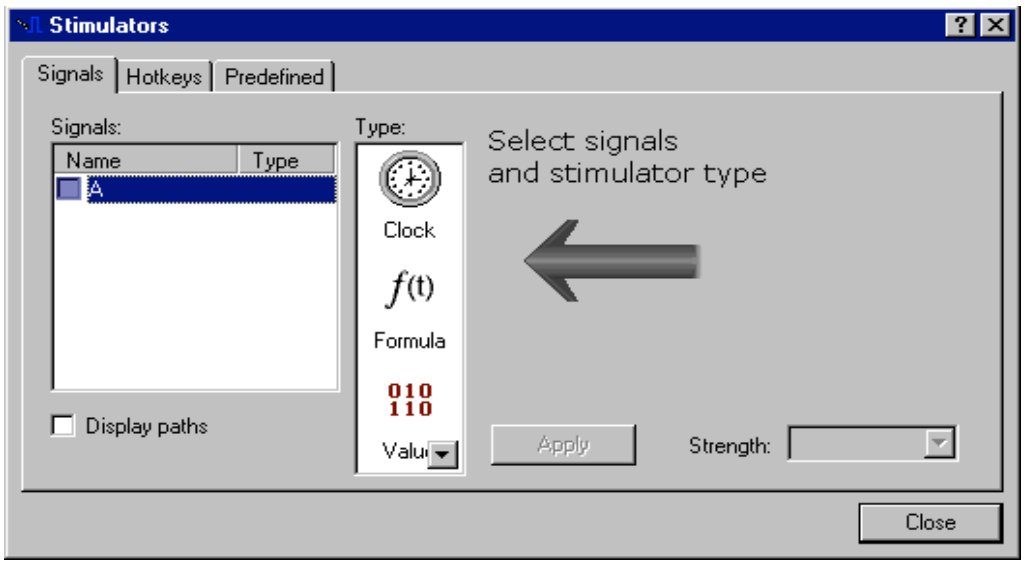


Figure 30

12. With the Stimulators window still opened, you can set additional signals by clicking the signals in the left side of the waveform. Once you have added the two input signals (i.e. A and B), choose a clock period of 10 ns for A by entering the

time in second box from the left at the top of the window (see Figure 31). Click the Apply button.

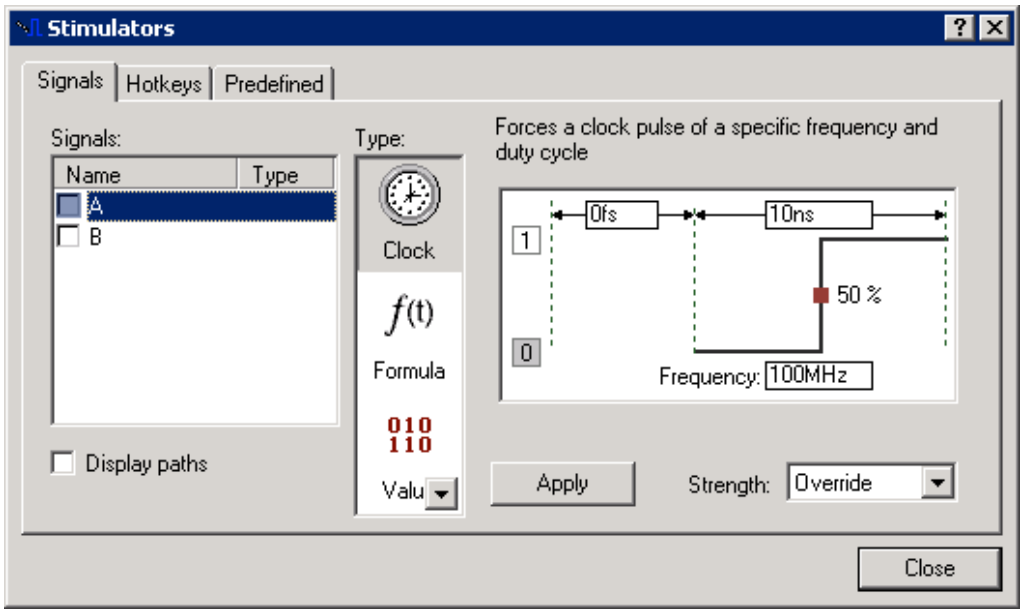


Figure 31

13. Select a clock with a period of 20 ns for input B.
14. When you are finished applying your stimulators, click the Close button.

At this point, you are ready to run the simulation using the waveform and stimulators.

1. The "Run For" field located in the Standard toolbar controls how long to run the simulation. You may change this by using the up and down arrows to the right of the field, or you may type in a time.

Figure 32

2. Click the Run For button in the Standard toolbar

Figure 33

3. To restart the simulation, click the Restart button in the Standard toolbar.

Figure 34

Note: if you make changes to the waveform by changing stimulators or adding/removing signals, you need to restart the simulation. Similarly, any change in the file means the file needs to be saved and recompiled prior to restarting the simulation. To end a simulation, simply click Simulation/End Simulation in the menu bar.

Figure 35 is an example of a simulation using the steps provided in this tutorial.

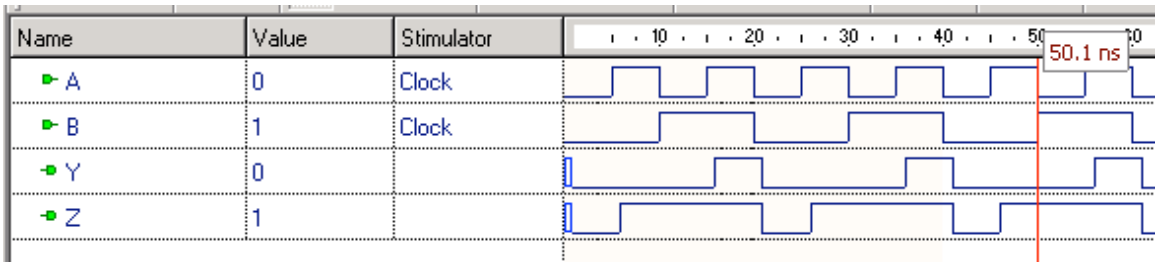


Figure 35

Now that you have ran a simulation and created a waveform, you should save that waveform. With the waveform tab active, press Ctrl-s to save, or right-click the tab and select save. Remember to use descriptive names. A good naming convention is <design name>_wv. You may have several waveforms for the same design. This is very useful in comparing different signal values and methods of driving the input signals. However, you should **close all waveforms** when you are done to avoid confusing signals when simulating other designs. You should experiment with the different methods available and save the results in separate waveforms for comparison; however, this is optional.

Concluding Remarks

This completes the first tutorial for Active-HDL there will be three other tutorials. Remember that this tutorial has only scratched the surface of the capabilities of this program. We strongly recommend you practice using the techniques described within this tutorial while experimenting with and exploring other methods and techniques that Active-HDL offers. Don't be discouraged if you do not understand what all of the tools are used for or the concepts the tutorial covers that have not yet been covered in class. By spending time with this tool and experimenting, you will save time by being better prepared for the more complicated upcoming assignments.