CSE352 Spring 2013 Homework Assignment #5 Solutions
Due in class Friday May 24th 2013

Read Harris & Harris 7.3 - Single Cycle Processor

Q1) Suppose that one of the following control signal in the single-cycle MIPS processor has a *stuck-at-0-fault*, meaning that the signal is always 0, regardless of its intended value. What instructions would malfunction? Why?

- RegWrite:
  - All R-type instructions, lw and addi:
    - The result of the operation/load/addition would not be written back to the destination register
- ALUOP[1] (also refer to Table 7.2 - ALU decoder truth table):
  - The following R-type instructions: add, sub, and, or, slt
    - With ALUOp stuck at 0, the ALU decoder would interpret all those instructions as either add or subtract operations. The ALUOp gets decoded to add or subtract depending on ALUOp[0].
- MemWrite:
  - Only sw is affected.
    - The memory write won't take place.

Instruction	Opcode	RegWrite	RegDst	ALUSrc	Branch	MemWrite	MemtoReg	ALUOp	Jump
R-type	000000	1	1	0	0	0	0	10	0
lw	100011	1	0	1	0	0	1	00	0
sw	101011	0	X	1	0	1	X	00	0
beq	000100	0	X	0	1	0	X	01	0
addi	001000	1	0	1	0	0	0	00	0
j	000010	0	X	X	X	0	X	XX	1

Exercise 7.1 - Consider instructions from table 7.5

Q2) Your friend is a crack circuit designer. She has offered to redesign one of the units in the single-cycle MIPS processor to have half the delay. Using the delays from Table 7.6, which unit should she work on to obtain the greatest speedup of the overall processor, and what would the cycle time of the improved machine be?

Element	Parameter	Delay (ps)
register clk-to-Q	t_{pcq}	30
register setup	t_{setup}	20
multiplexer	t_{mux}	25
ALU	t_{ALU}	200
memory read	t_{mem}	250
register file read	t_{RFread}	150
register file setup	$t_{RFsetup}$	20

Equation 7.3:

$$T_c = t_{pcq\_PC} + 2t_{mem} + t_{RFread} + 2t_{mux} + t_{ALU} + t_{RFsetup}$$

Based on equation 7.3 and table 7.5, the memory unit dominates the cycle time.

By halving t_{mem} to 125ps, we can reduce Tc from 950ps to 700ps.