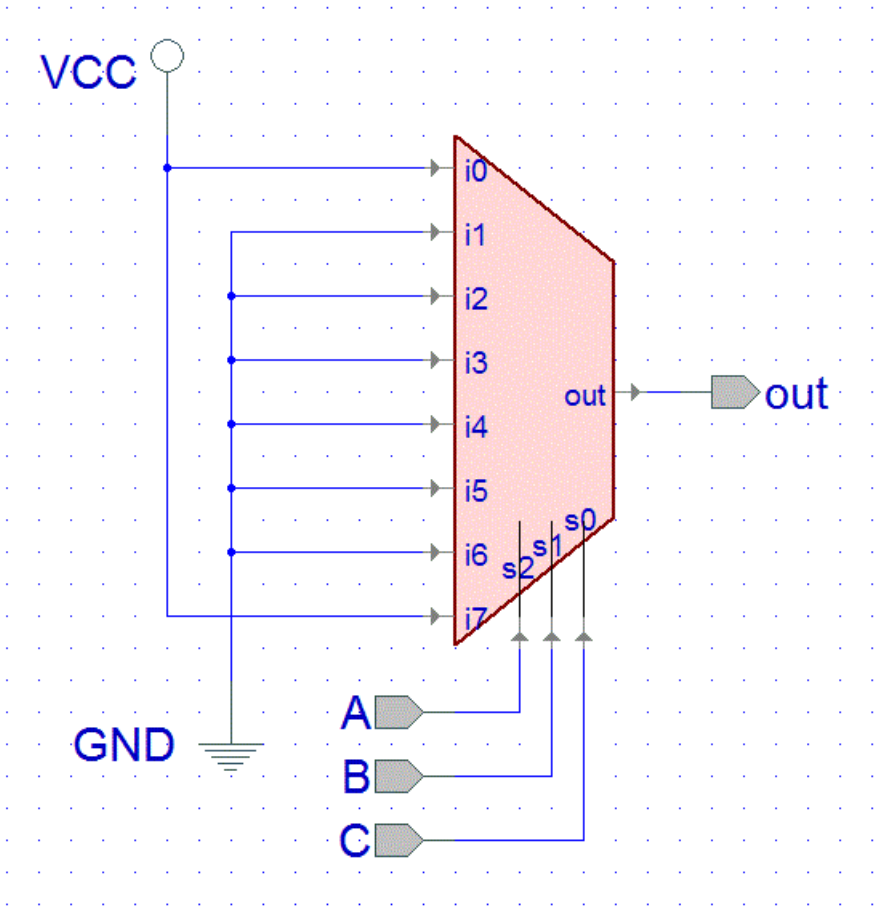
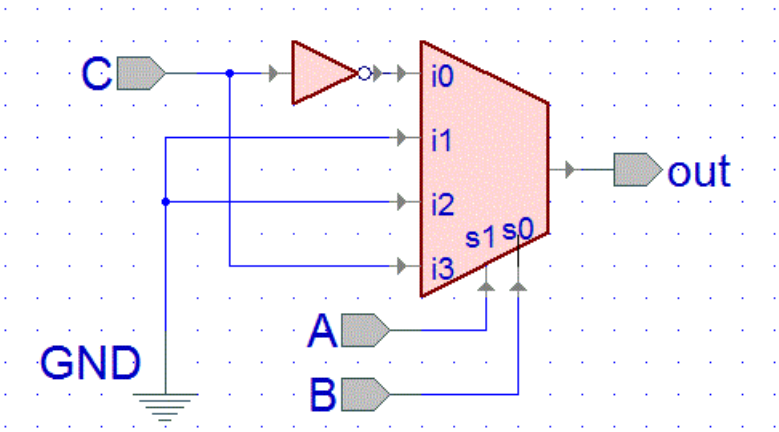
CSE 352 A Homework 3 solutions

Question 1:

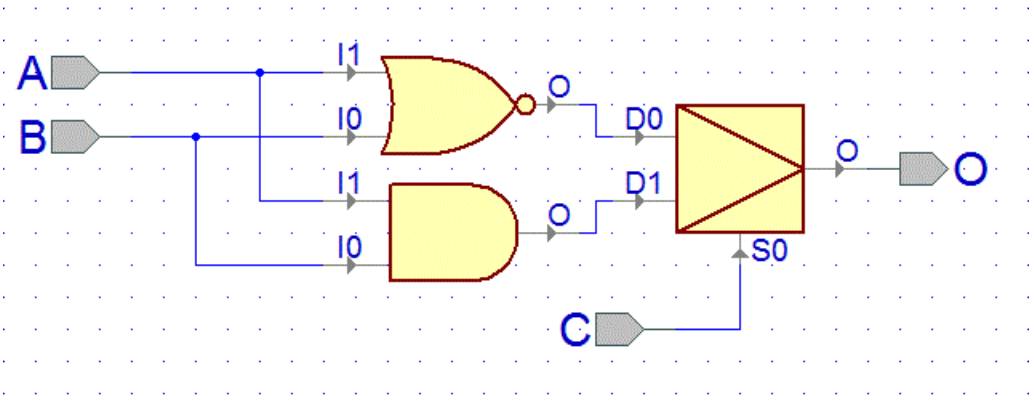
Part A:



Part B:

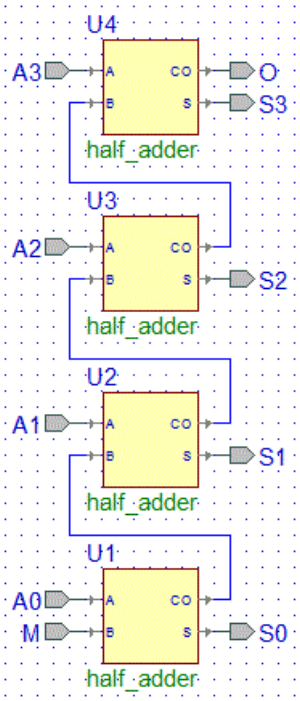


Part C:



Question 2:

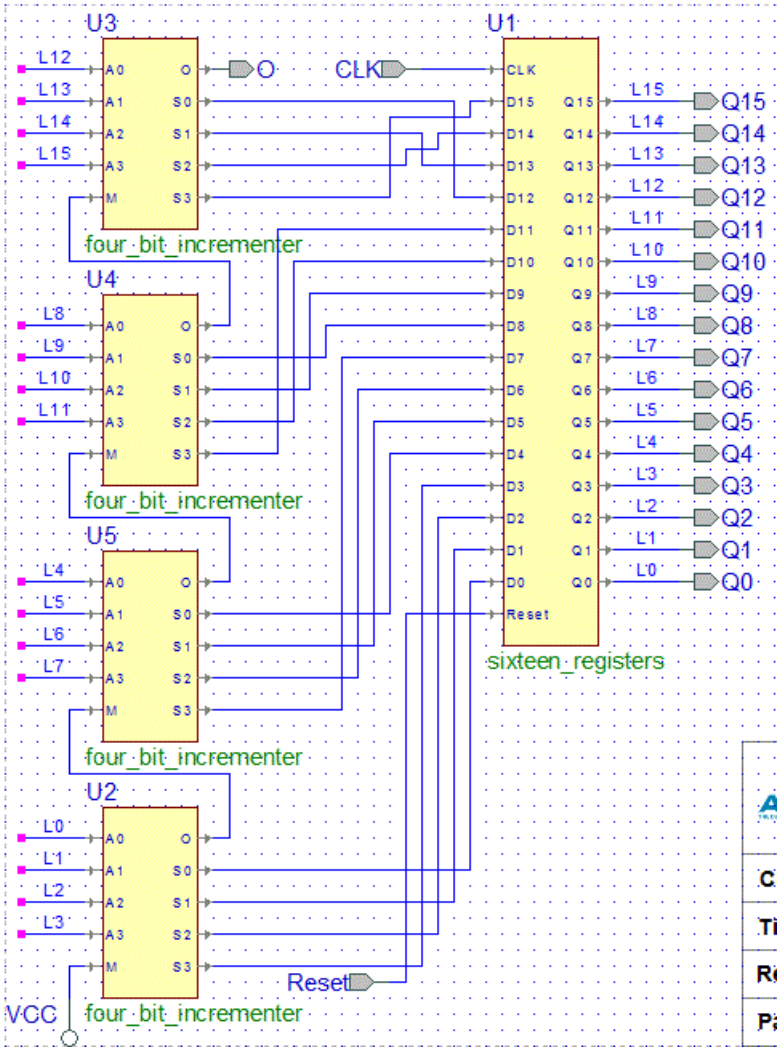
Incrementer:



REVISED:

Delay question: The critical path is from A0/M to S3. This path goes through 3 AND gates (from the first three adders), and an XOR gate (from the last adder). This adds up to: 3*0.5 + 1.5 = 3ns.

16-bit counter: (see next page)


U3
U1
U4
U5
U2
four_bit_incrementer
sixteen_registers
CLK
O
Reset
VCC
L12
L13
L14
L15
L8
L9
L10
L11
L4
L5
L6
L7
L0
L1
L2
L3
A0
A1
A2
A3
M
S0
S1
S2
S3
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
Q15
Q14
Q13
Q12
Q11
Q10
Q9
Q8
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0