CSE352 Spring 2013 Homework Assignment #2
Due in class Monday April 22nd 2013

Solutions

Q1) Timing diagrams

a) A circuit composed of AND and NAND gates is given in Fig. 1. The delay of an AND gate is 3ns, and the delay of a NAND gate is 2ns. Complete Fig. 2 given the waveforms of inputs A, B, C, D. Note that the circuit before t=0 is at steady state. The timescale of this waveform is in ns.

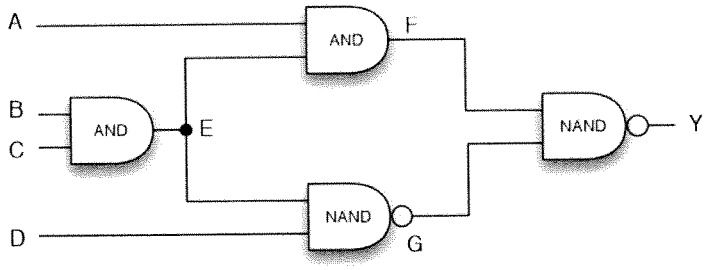

Figure 1: Circuit schematic

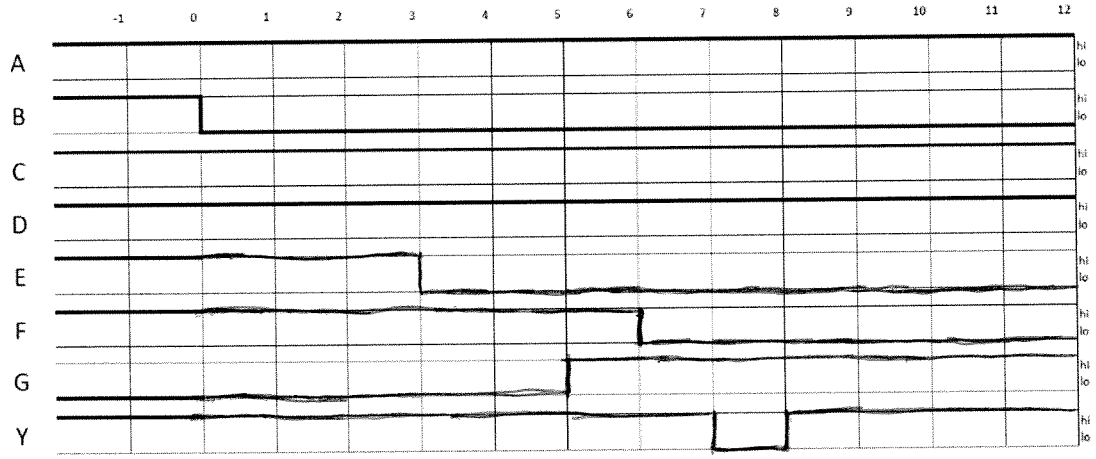

Figure 2: Waveform for part 2

b) The engineer that designed this circuit might not have accounted for glitches. Suggest adding delay to one gate to fix the glitch issue. Which gate would it be, and what delay would this gate now have? Add delay to the NAND gate at point G. so that total delay is 3ns rather than 2ns

c) Complete the Waveform on Fig. 3 for this new glitch-free circuit.

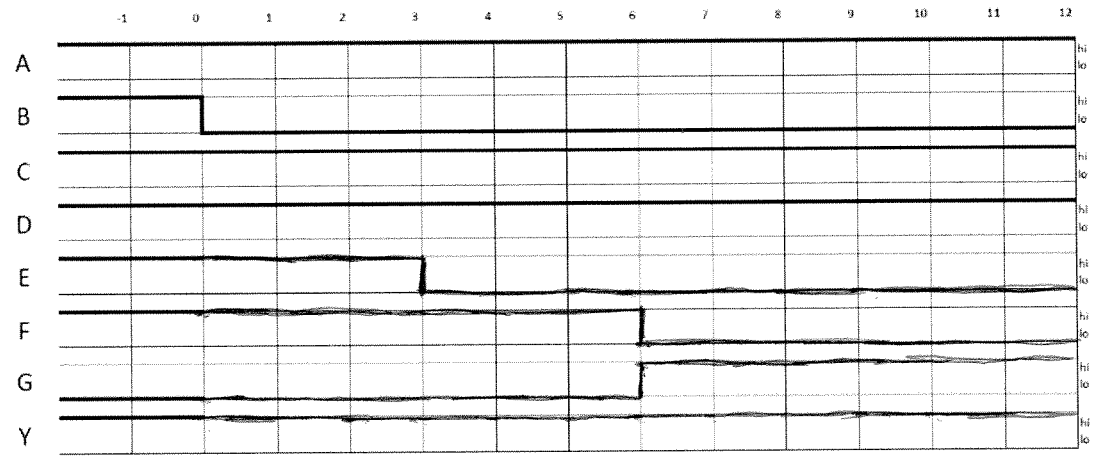

Figure 3: Waveform for part c

Q3) Latches

Given the negative-edge triggered D flip-flop (composed of cascaded gated D latches) in Fig 4. and the input pattern of input D, complete the output waveform for the intermediate value X and the output Q.
Make the following assumptions:

- We can assume that each latch has 0 delay.
- Ignore setup/hold time requirements.
- If a D latch "captures" an input when it is transitioning from lo-to-hi or hi-to-lo, the output value will be lo and hi respectively (value before the transition is latched).

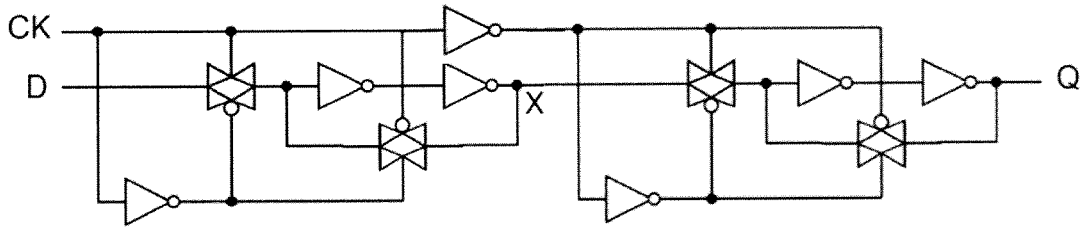

Figure 4: Neg-edged flip flop

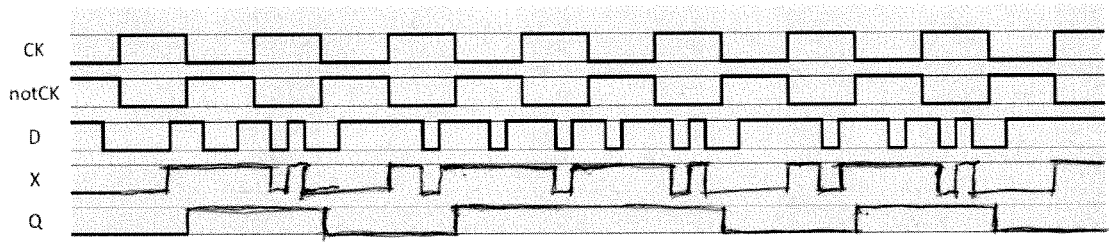

Figure 5: Waveform

X is same as D when CK is high
Q is same as X when notCK is high