Caches II

CSE 351 Autumn 2024

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Relevant Course Information

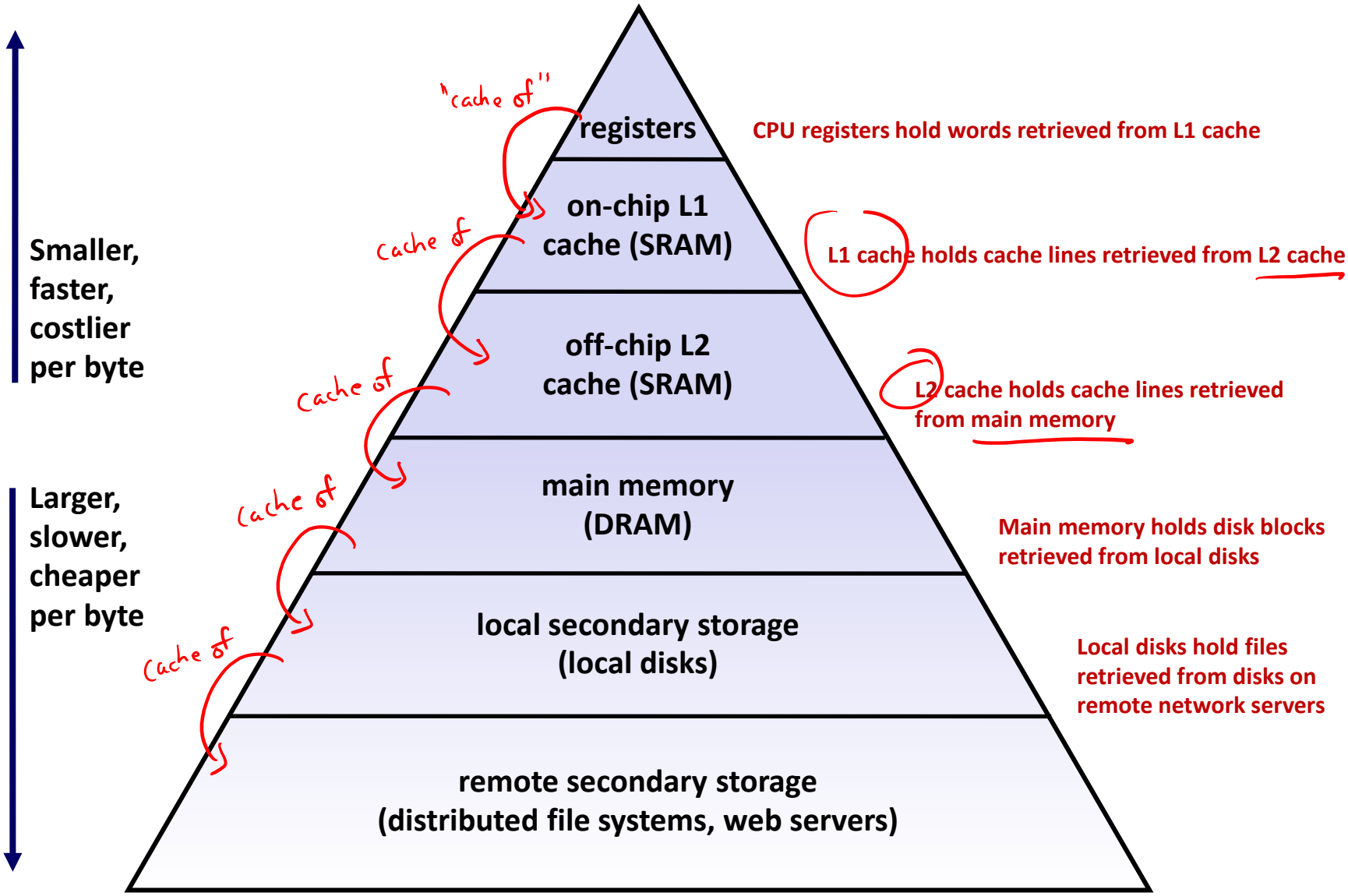
- HW15 due TONIGHT, Monday (11/04) @ 11:59 pm
- HW16 due Wednesday (11/06) @ 11:59 pm
- Lab 3 due Mon 11/11
  - Encouraged to aim for Fri 11/08, actual deadline Mon 11/11
  - You have everything you need to do the lab as of 10/28
  - Last part of HW15 is useful for Lab 3
- Mid-quarter Survey due Saturday (11/09)

Memory Hierarchies (Review)

- Some fundamental and enduring properties of hardware and software systems:
  - Faster storage technologies almost always cost more per byte and have lower capacity
  - The gaps between memory technology speeds are widening
    - True for: registers ↔ cache, cache ↔ DRAM, DRAM ↔ disk, etc.
  - Well-written programs tend to exhibit good locality

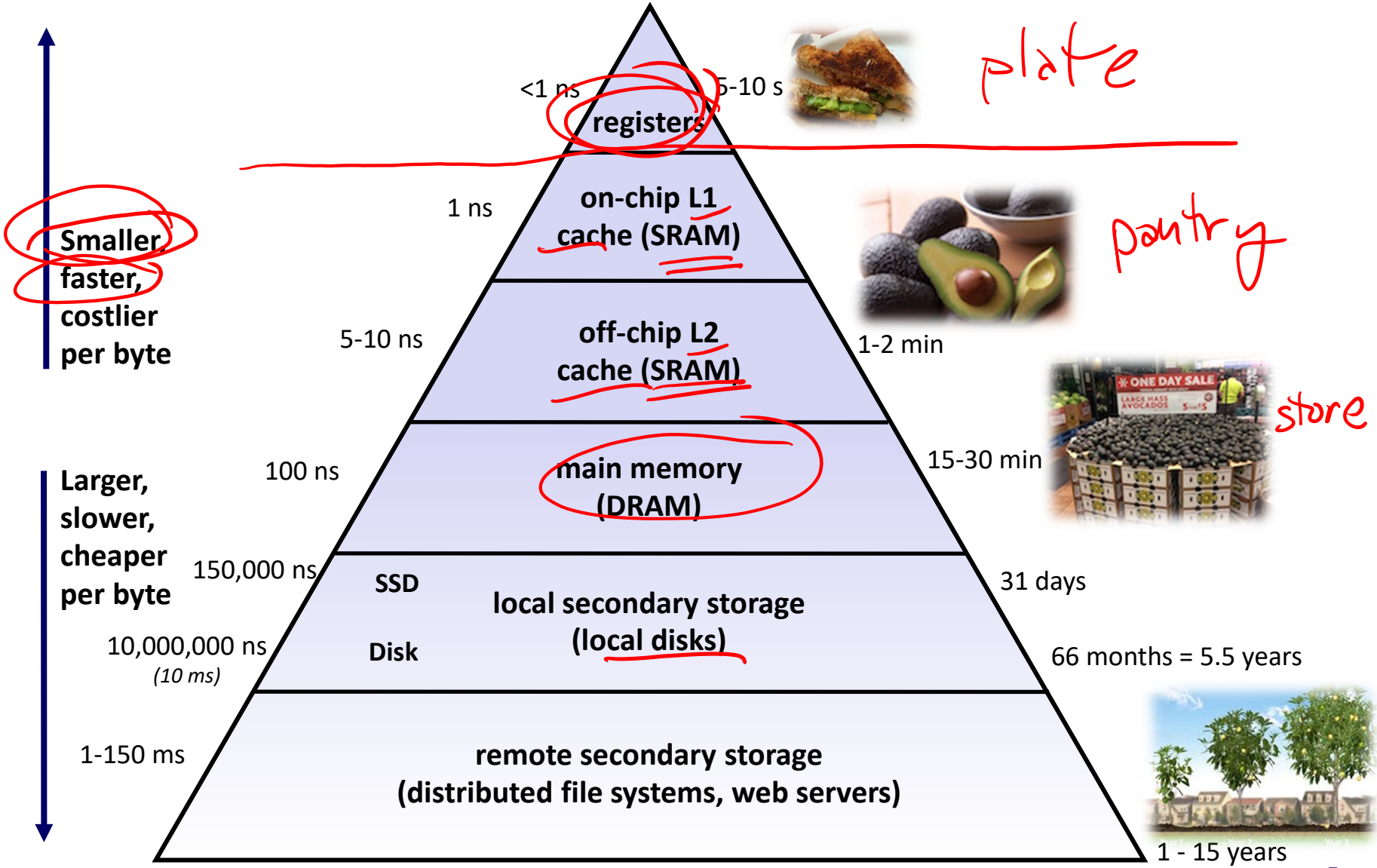
- These properties complement each other beautifully
  - They suggest an approach for organizing memory and storage systems known as a memory hierarchy
    - For each level *x*, the faster, smaller device at level x serves as a cache for the larger, slower device at level x+1

An Example Memory Hierarchy (1)

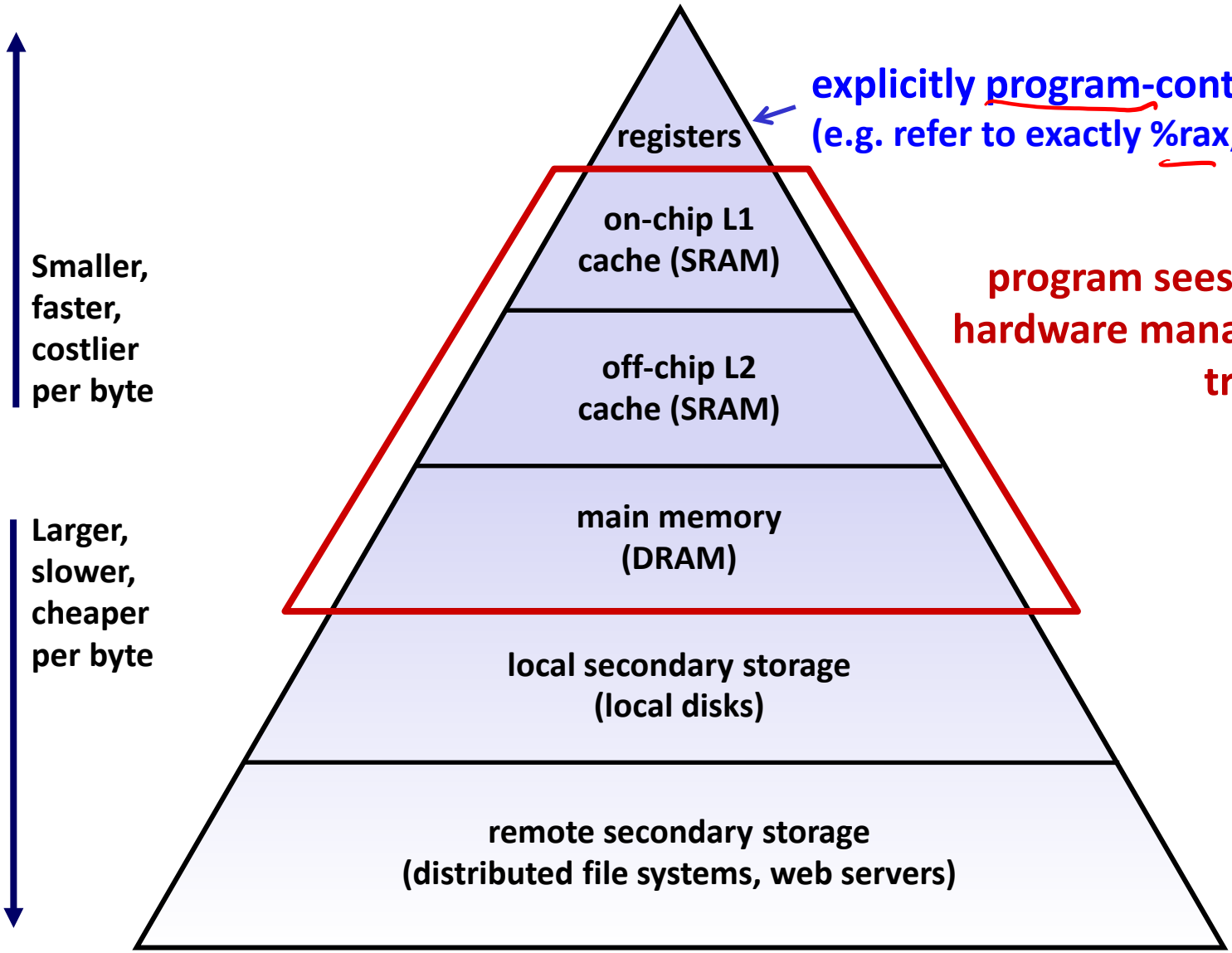


addq %rax, (%rbx)

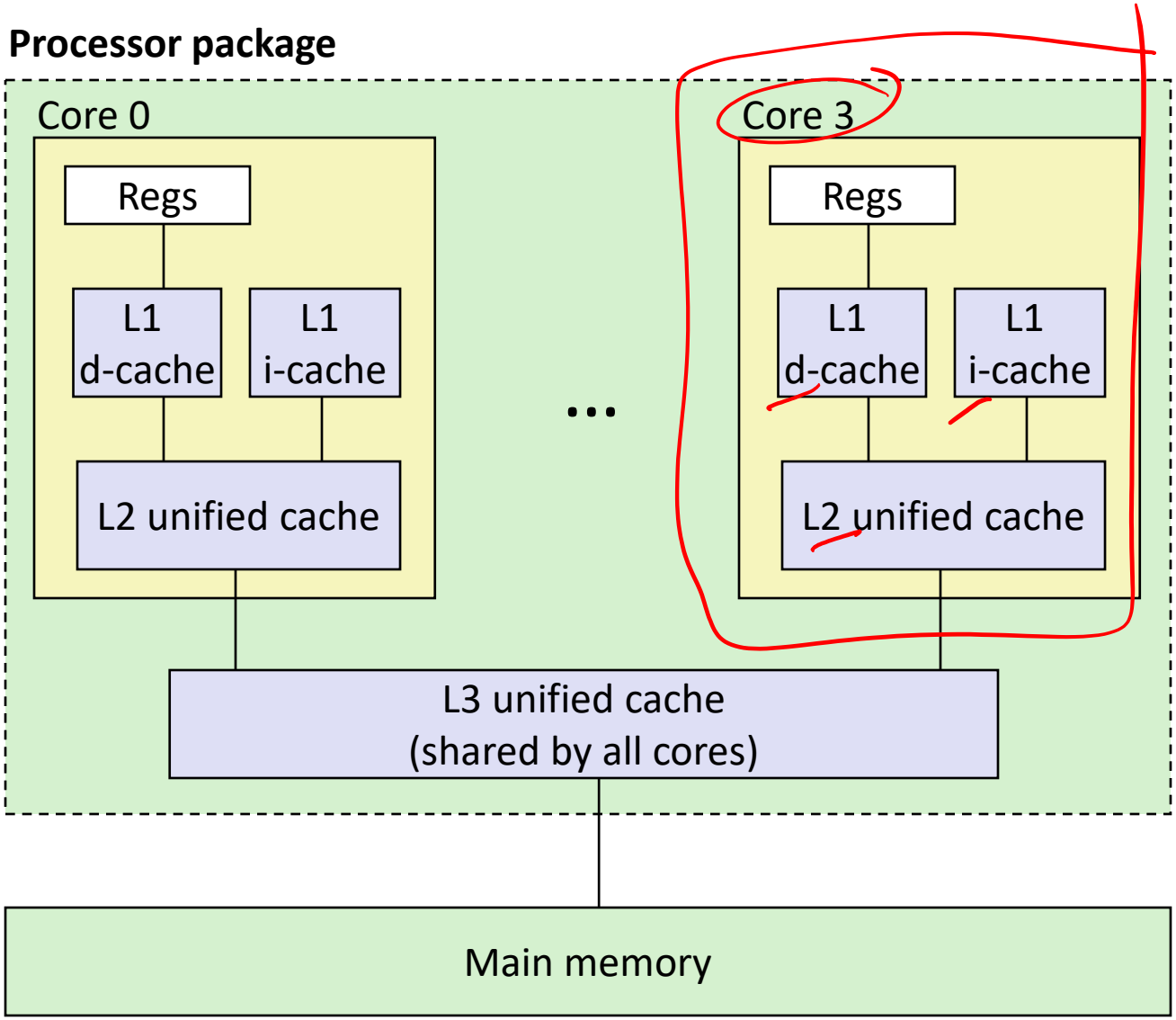
An Example Memory Hierarchy (2)



Registers vs. Memory



Intel Core i7 Cache Hierarchy



Block size:
64 bytes for all caches

L1 i-cache and d-cache:
32 KiB, 8-way,
Access: 4 cycles

L2 unified cache:
256 KiB, 8-way,
Access: 11 cycles

L3 unified cache:
8 MiB, 16-way,
Access: 30-40 cycles

Making memory accesses fast!

- Cache basics
- Principle of locality
- Memory hierarchies
- **Cache organization**
  - **Direct-mapped (*sets*; index + tag)**
  - Associativity (ways)
  - Replacement policy
  - Handling writes
- Program optimizations that consider caches

Reading Review

- Terminology:
  - Memory hierarchy
  - Cache parameters: block size (K), cache size (C)
  - Addresses: block offset field (k bits wide)
  - Cache organization: direct-mapped cache, index field

Review Questions

- We have a direct-mapped cache with the following parameters:
  - Block size of 8 bytes $K = 2^3$ B
  - Cache size of 4 KiB $C = 2^{12}$ B
    2^2 KiB $= 2^{10}$ B
- How many blocks can the cache hold? $C/K = \frac{2^{12}}{2^3} = 2^9 = 512$ blocks
- How many bits wide is the block offset field? $\log_2 K = 3$ bits
- Which of the following addresses would fall under block number 3?

A. 0x3 $\lfloor 3/8 \rfloor = 0$ 0b...000011 block 0

B. 0x1F $\lfloor 31/8 \rfloor = 3$ 0b...011111 block 3

C. 0x30 $\lfloor 48/8 \rfloor = 6$ 0b...110000 block 6

D. 0x38 $\lfloor 56/8 \rfloor = 7$ 0b...111000 block 7

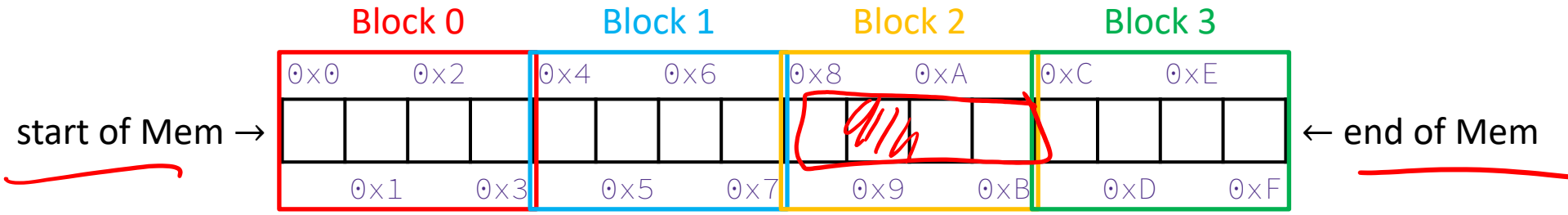
Block Size (1)

Note: The textbook uses "B" for block size

- Block Size (K): unit of transfer between \$ and Mem
  - Given in bytes and always a power of 2 (*e.g.*, 64 B)
  - Blocks consist of adjacent bytes (differ in address by 1)
    - Spatial locality!

Block size

- Small example ($K = 4$ B):

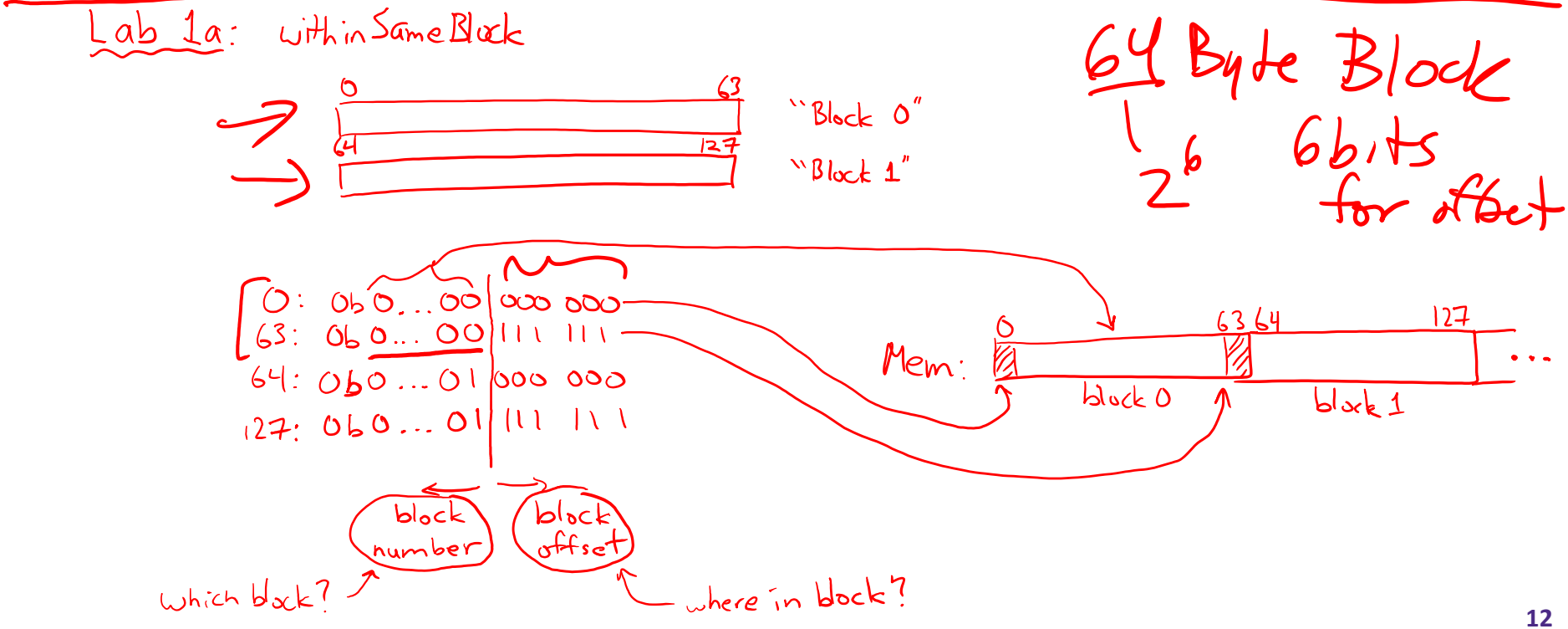


Address Space = 16 bytes

Block Size (2)

Note: The textbook uses "B" for block size

- Block Size (K): unit of transfer between $ and Mem
  - Given in bytes and always a power of 2 (*e.g.*, 64 B)
  - Blocks consist of adjacent bytes (differ in address by 1)
    - Spatial locality!



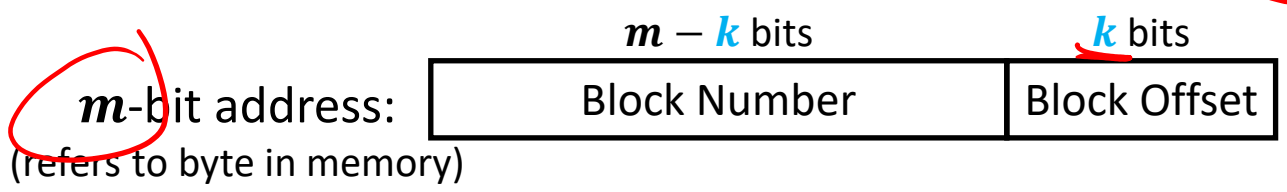
Block Size (3)

Note: The textbook uses "b" for offset bits

- Block Size (K): unit of transfer between $ and Mem
  - Given in bytes and always a power of 2 (*e.g.*, 64 B)
  - Blocks consist of adjacent bytes (differ in address by 1)
    - Spatial locality!

- Offset field
  - Low-order $\log_2(K) = \boldsymbol{k}$ bits of address tell you which byte within a block
    - (address) mod 2^n = n lowest bits of address
  - (address) modulo (# of bytes in a block)

How many bits do I need to specify every byte in a block?

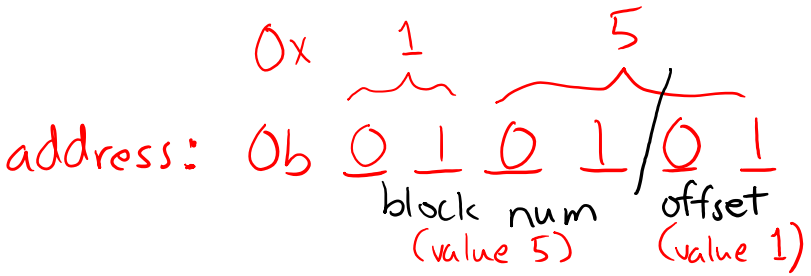


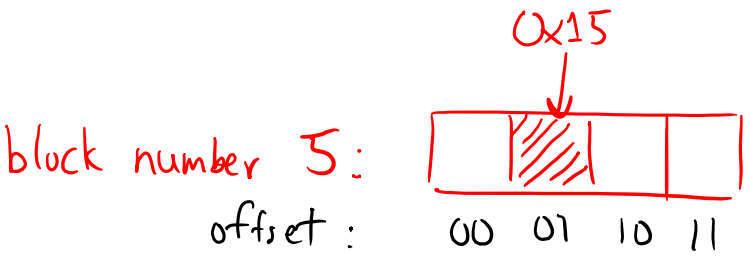
Block Size (4)

Note: The textbook uses "b" for offset bits

- Block Size (K): unit of transfer between $ and Mem
  - Given in bytes and always a power of 2 (*e.g.*, 64 B)
  - Blocks consist of adjacent bytes (differ in address by 1)
    - Spatial locality!

- Example:
  - If we have 6-bit addresses (m) and block size K = 4 B, which block and byte does `0x15` refer to?





offset width = $\log_2(K) = \log_2(4) = 2$ bits

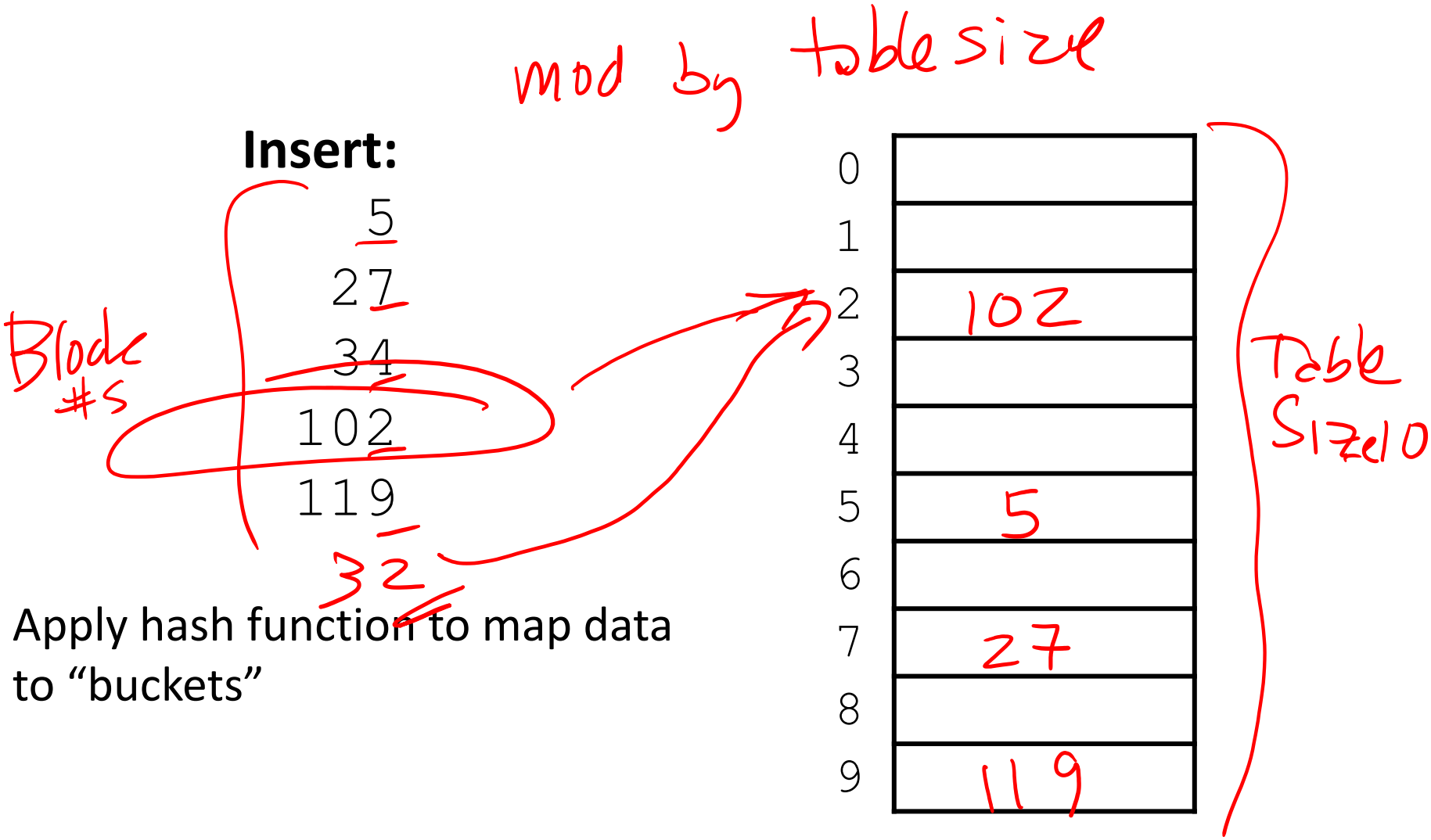
Cache Size

- Cache Size (C): amount of *data* the $ can store
  - Cache can only hold so much data (subset of next level)
  - Given in bytes (C) or number of blocks (C/K)
  - Example: C = 32 KiB = 512 blocks if using 64-B blocks

$2^5 \times 2^{10} = 2^{15}$ B $\times \frac{1 \text{ block}}{2^6 \text{ B}} = 2^9$ blocks

- Where should data go in the cache?
  - We need a mapping from memory addresses to specific locations in the cache to make checking the cache for an address **fast**
- What is a data structure that provides fast lookup?
  - Hash table!

Hash Tables for Fast Lookup



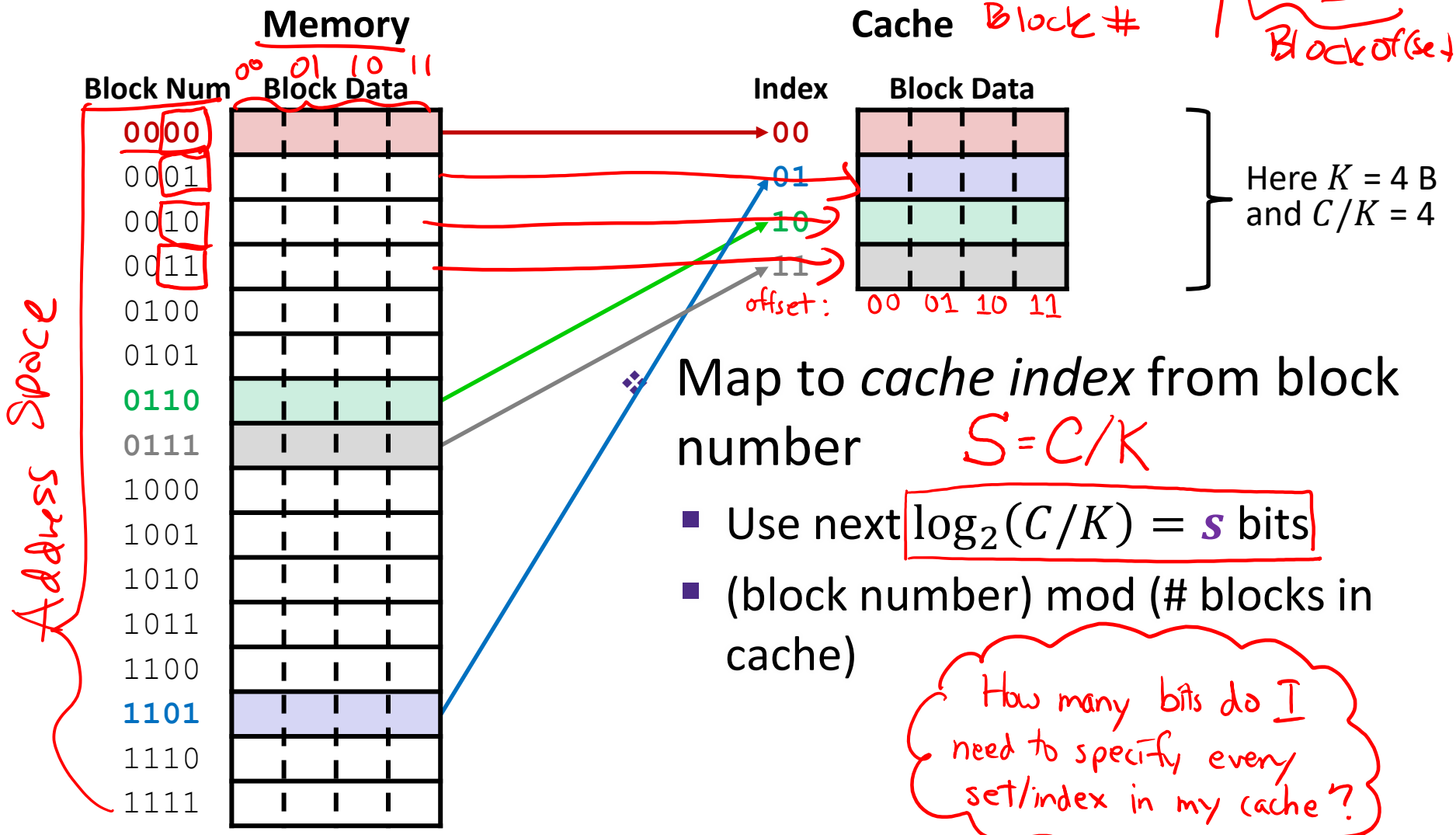
Apply hash function to map data to "buckets"

Cache Size C = 16 Bytes K = Block Size = 4 Bytes

Place Data in Cache by Hashing Address

Addresses are 6 bits 0b _ _ _ _ / _ _

Block # | Block offset



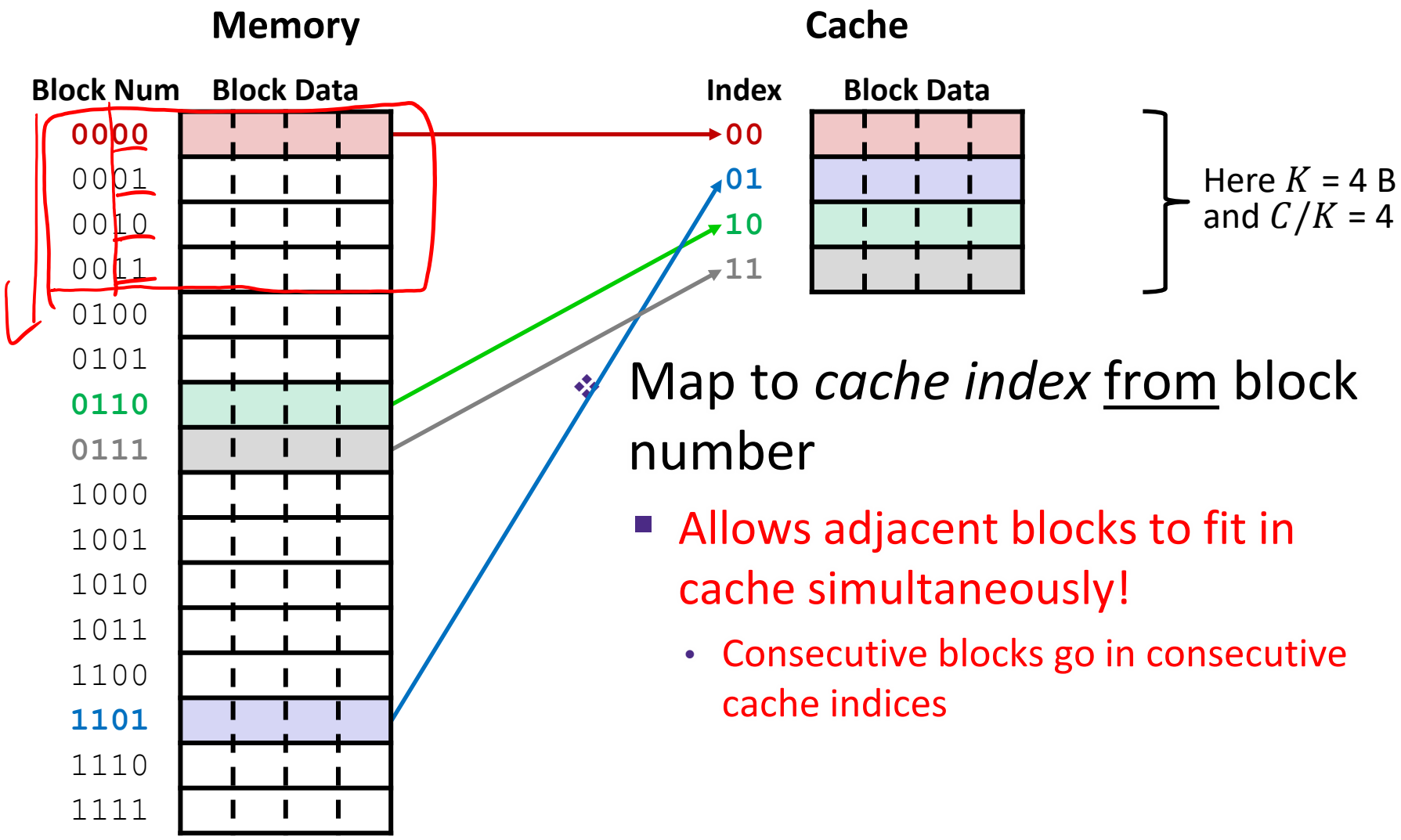
Map to *cache index* from block number

S = C/K

- Use next $\log_2(C/K) = s$ bits
- (block number) mod (# blocks in cache)

How many bits do I need to specify every set/index in my cache?

Place Data in Cache by Hashing Address

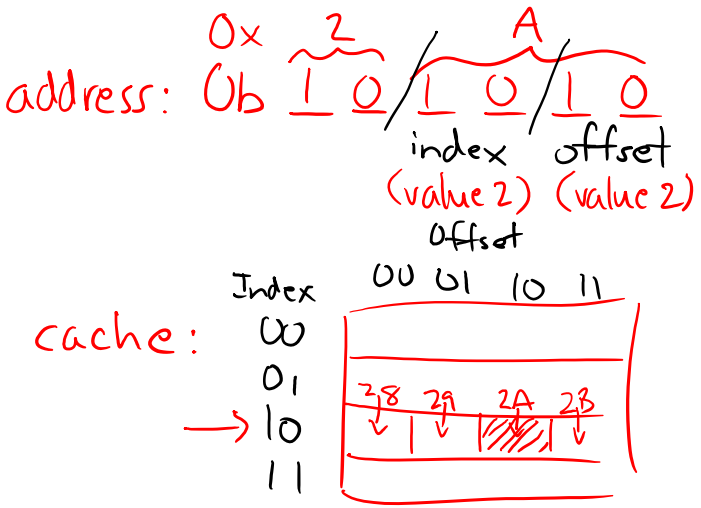


Map to *cache index* from block number

- Allows adjacent blocks to fit in cache simultaneously!
  - Consecutive blocks go in consecutive cache indices

Polling Question

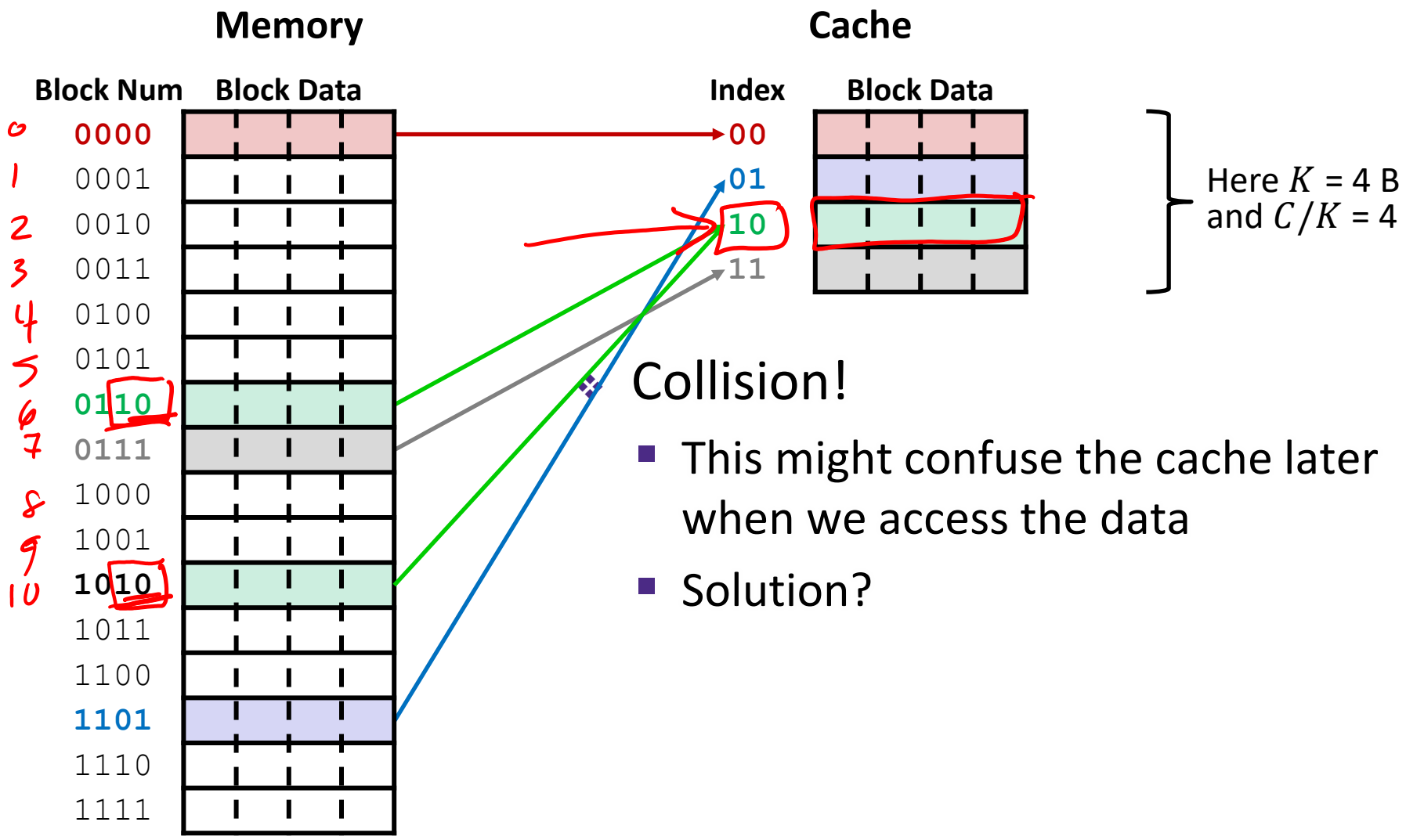
- 6-bit addresses, block size K = 4 B, and our cache holds S = 4 blocks. (m; $= C/K$, $s = \log_2(4) = 2$ bits)
- A request for address **0x2A** results in a cache miss. Which index does this block get loaded into and which 3 other addresses are loaded along with it?
  - Vote on Ed Lessons



Index 2 (0b10)

along with: 0b1010 00 = 0x28
01 = 0x29
11 = 0x2B

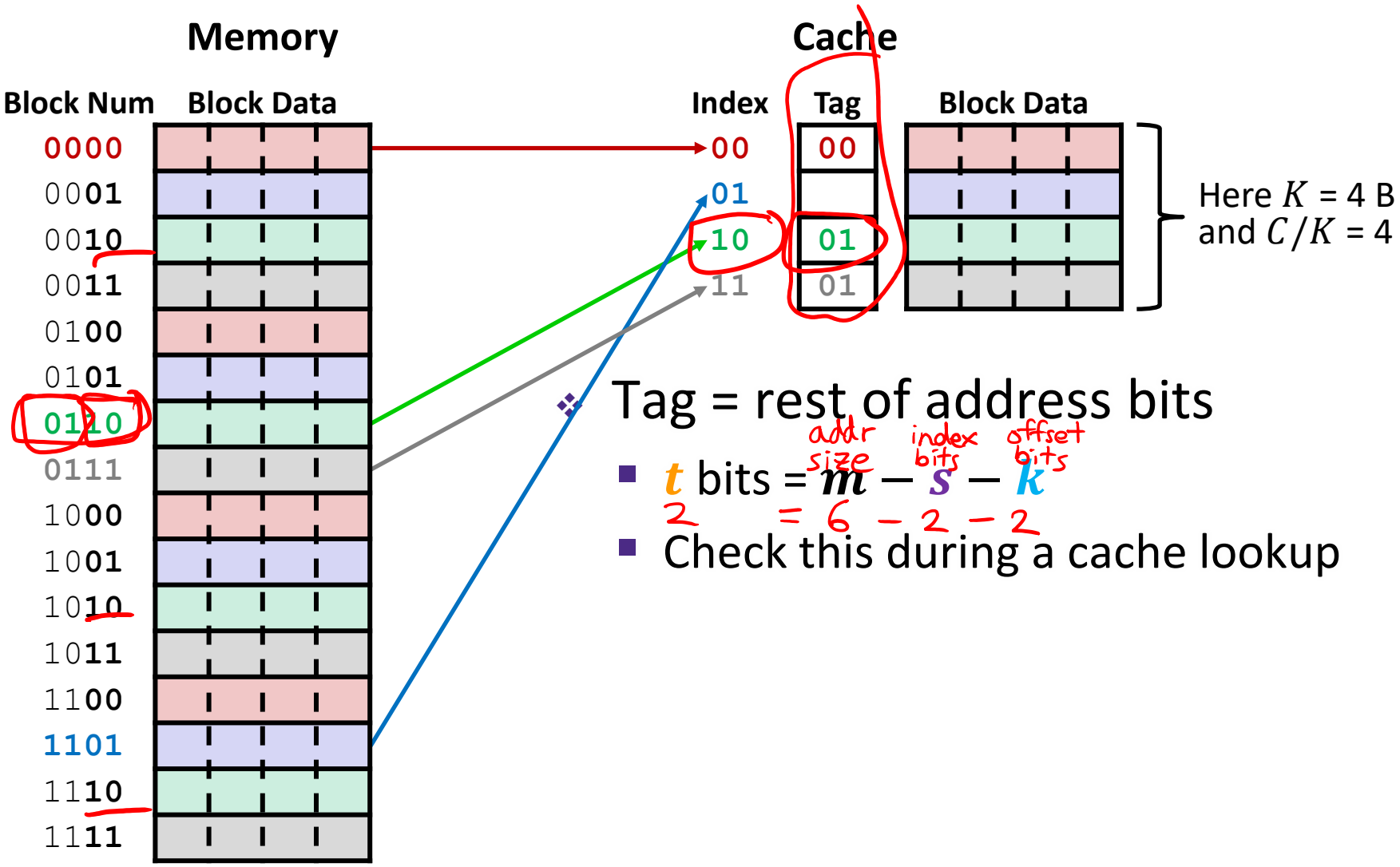
Place Data in Cache by Hashing Address



Collision!

- This might confuse the cache later when we access the data
- Solution?

Tags Differentiate Blocks in Same Index



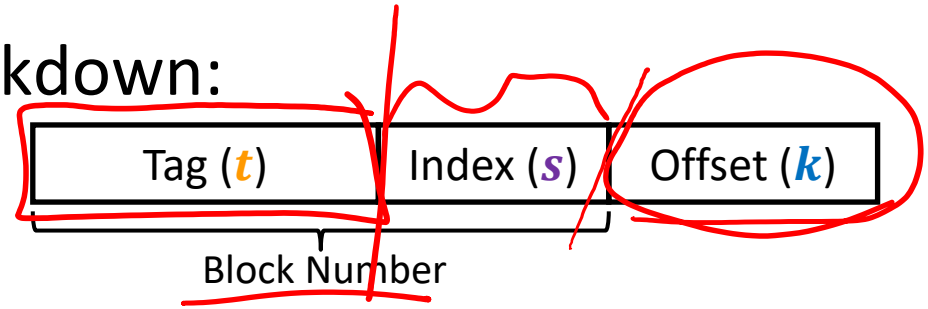
Tag = rest of address bits

- t bits = $m - s - k$ (addr size, index bits, offset bits)
  - $t = 6 - 2 - 2$
- Check this during a cache lookup

Checking for a Requested Address

- CPU sends address request for chunk of data
  - Address and requested data are not the same thing!
    - Analogy: your friend ≠ their phone number

- TIO address breakdown:



1. **Index** field tells you where to look in cache
2. **Tag** field lets you check that data is the block you want
3. **Offset** field selects specified start byte within block

- **Note:** t and s sizes will change based on hash function

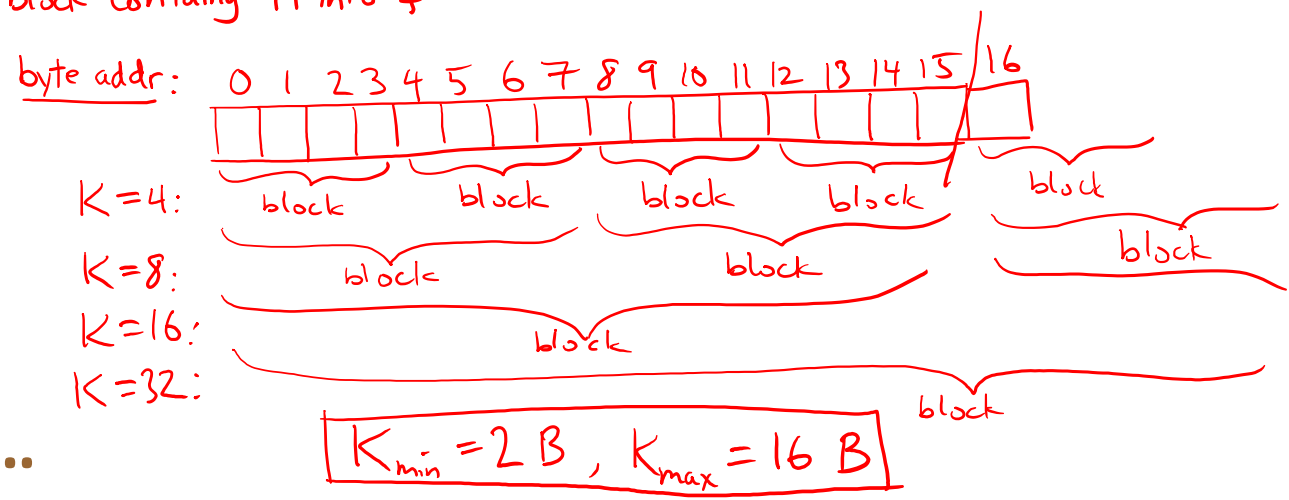
Cache Puzzle

- Based on the following behavior, which of the following block sizes is NOT possible for our cache?
  - Cache starts *empty*, also known as a *cold cache*
  - Access (addr: hit/miss) stream:
    - (14: miss), (15: hit), (16: miss)
- [Not in Ed Lessons]

hit: block with data already in $
miss: data not in $, pulls block containing data from Mem

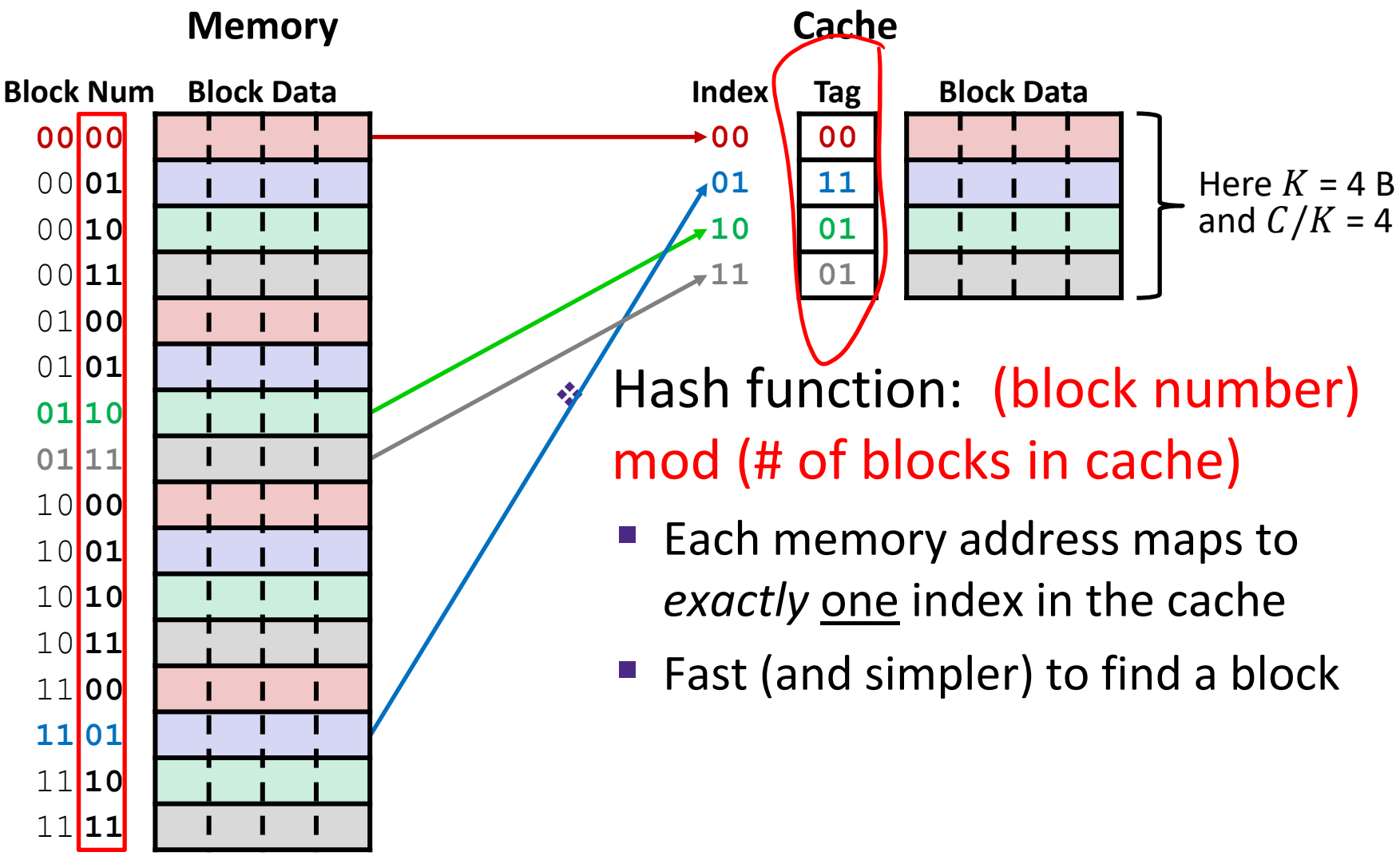
↳① pulls block containing 14 into $
↳② 14 & 15 are in the same block
↳③ 16 is in a different block

A. 4 bytes
B. 8 bytes
C. 16 bytes
D. 32 bytes
E. We're lost…



$K_{min} = 2\,B$, $K_{max} = 16\,B$

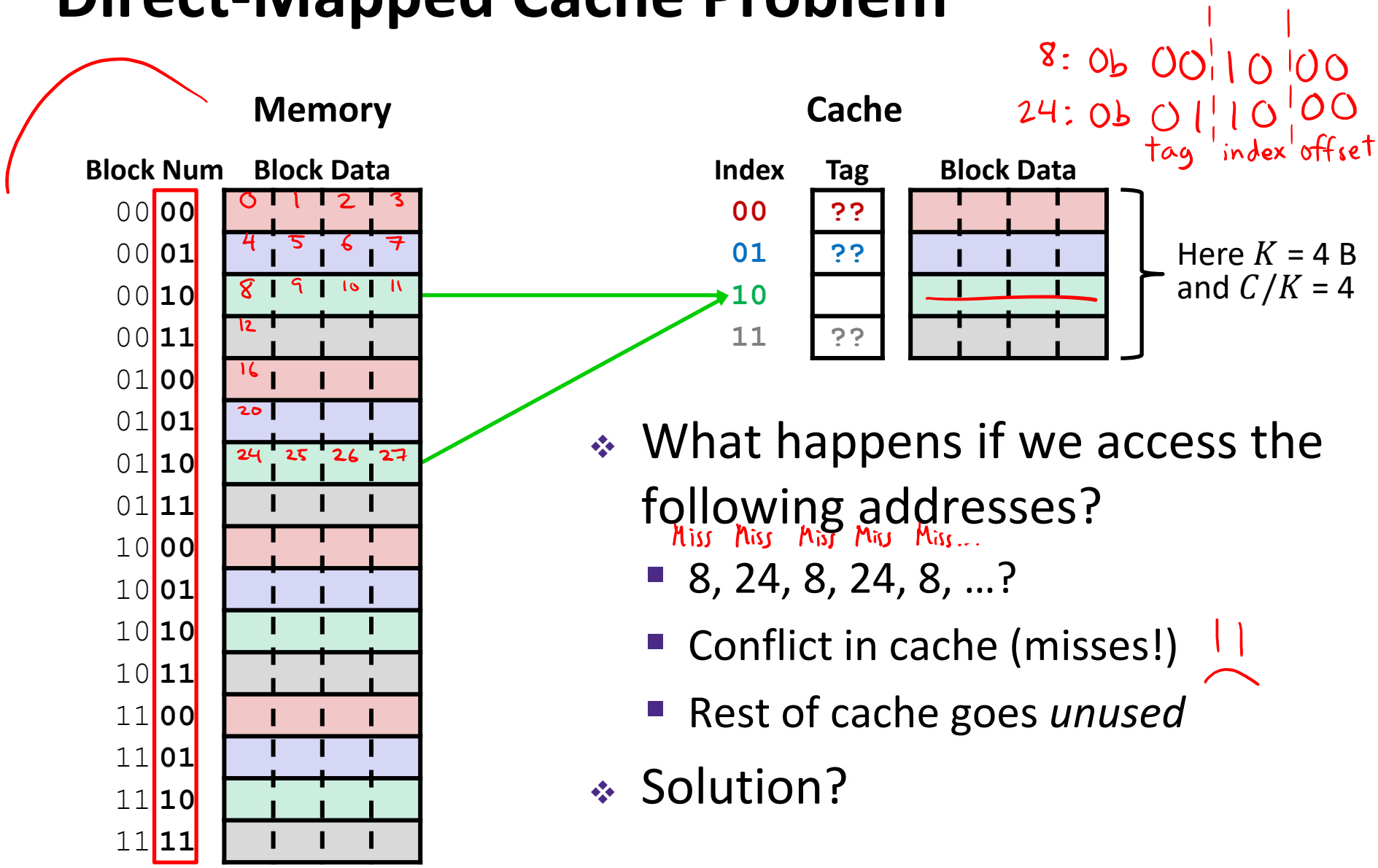
Summary: Direct-Mapped Cache



Hash function: (block number) mod (# of blocks in cache)

- Each memory address maps to *exactly* one index in the cache
- Fast (and simpler) to find a block

Direct-Mapped Cache Problem



- What happens if we access the following addresses? Miss Miss Miss Miss Miss...
  - 8, 24, 8, 24, 8, …?
  - Conflict in cache (misses!)
  - Rest of cache goes *unused*
- Solution?