Virtual Memory Overview

Virtual address (VA): What your program uses

Virtual Page Number	Virtual Page Offset

Physical address (PA): Where you actually go in physical memory

Physical Page Number	Physical Page Offset

Pages

A large chunk of memory or disk with a fixed size. Two addresses within the same virtual page get mapped to addresses in the same physical page. The page table determines the mapping.

The Page Table

Index = VPN (not stored)	**Page Valid**	**Permission Bits (read, write, ...)**	**Physical Page Number (PPN)**
0			
1			
2			
…			
Max VPN			

Each stored row of the page table is called a **page table entry** (the grayed section is the first page table entry). The page table is stored *in memory*; the OS sets the **page table base register** to the address of the first entry of the page table for the current process. The OS tracks dirty pages to know whether updating a page on disk is necessary. Each process gets its own page table.

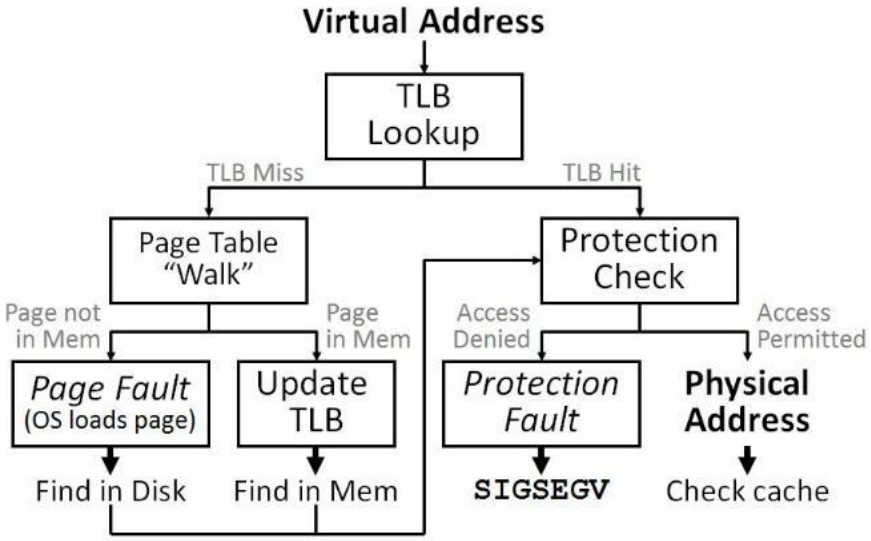
The Translation Lookaside Buffer (TLB)

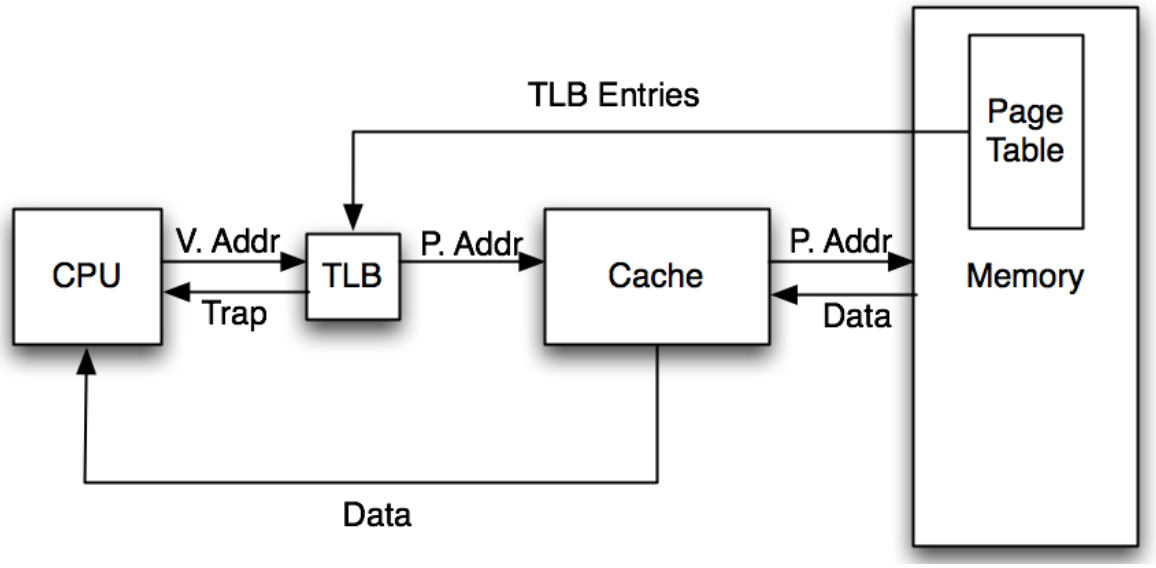
A cache for the page table. Each "block" is a single page table entry. If an entry is not in the TLB, it's a TLB miss and the PTE is requested from the page table. A typical TLB entry looks like:

TLB Tag	Page Table Entry		
	Page Valid	Permission Bits	Physical Page Number
…	…	…	…

It is the VPN that is split into TLB Tag (TLBT) and TLB Index (TLBI) based on how many sets are in the TLB. The TLB ignores the page offset because it is not part of the VPN → PPN translation.

The Big Picture: Logical Flow





1) VA → PA translation is done by the MMU using the TLB and the page table
   - Achieved by looking up VPN → PPN mapping in PTE, then joining PPN to PPO
2) PA is used to access the cache
   - Even though it uses the same bits, this is a *different* field split (`T|I|O` vs. `PPN|PPO`)
3) Data is returned to CPU from the cache or physical memory

Virtual Memory Acronyms and Definitions

VA	Virtual Address
VPN	Virtual Page Number
VPO	Virtual Page Offset
PT	Page Table
PTBR	Page Table Base Register
TLBT	TLB Tag
MMU	Memory Management Unit

PA	Physical Address
PPN	Physical Page Number
PPO	Physical Page Offset
PTE	Page Table Entry
TLB	Translation Lookaside Buffer
TLBI	TLB Index

TLB Hit	PTE for requested VPN is currently in the TLB – this page was used recently
TLB Miss	PTE for requested VPN not currently in the TLB – must look for in PT
Page Table Hit	PPN mapping for requested VPN in PT – page currently resides in physical memory
Page Fault	PTE is invalid – page must be allocated or paged in from disk
Protection Fault	PTE for requested VPN has permission bits that prohibit the specified operation
Page In	When the OS moves a page of data from disk to physical memory
Page Out	When the OS copies a page from physical memory to disk – only done when dirty
Thrashing	Frequent paging in and out due to insufficient physical memory that eats up a significant amount of CPU time
Context Switch	Switching between processes – storing the state of the current process and then restoring the state of the next process, including all register values (including the PTBR and program counter) and invalidating the TLB entries
Swap Space	Temporary space allocated in your disk to hold data that is paged out from the currently running processes