

# x86-64 Programming II

CSE 351 Spring 2022

## Instructor:

Ruth Anderson

## Teaching Assistants:

Melissa Birchfield

Jacob Christy

Alena Dickmann

Kyrie Dowling

Ellis Haker

Maggie Jiang

Diya Joy

Anirudh Kumar

Jim Limprasert

Armin Magness

Hamsa Shankar

Dara Stotland

Jeffery Tian

Assaf Vayner

Tom Wu

Angela Xu

Effie Zheng



<http://xkcd.com/99/>

# Relevant Course Information

- ❖ hw7 due TONIGHT (4/15) @ 11:59 pm
- ❖ Lab 1b, due Monday 4/18
  - Submit `aisle_manager.c`, `store_client.c`, and `lab1Bsynthesis.txt`
- ❖ Lab 2 (x86-64) coming soon!
  - Learn to read x86-64 assembly and use GDB
- ❖ Midterm:
  - Released Mon 5/2 11:59pm, due Wed 5/4 11:59pm
  - Take home, Individual but some discussion permitted
  - More details later

# Extra Credit

- ❖ All labs starting with Lab 2 have extra credit portions
  - These are meant to be fun extensions to the labs
- ❖ Extra credit points *don't* affect your lab grades
  - From the course policies: “they will be accumulated over the course and will be used to bump up borderline grades at the end of the quarter.”
  - Make sure you finish the rest of the lab before attempting any extra credit

# Example of Basic Addressing Modes

```
void swap(long* xp, long* yp)
{
    long t0 = *xp;
    long t1 = *yp;
    *xp = t1;
    *yp = t0;
}
```

```
swap:
    movq    (%rdi), %rax
    movq    (%rsi), %rdx
    movq    %rdx, (%rdi)
    movq    %rax, (%rsi)
    ret
```

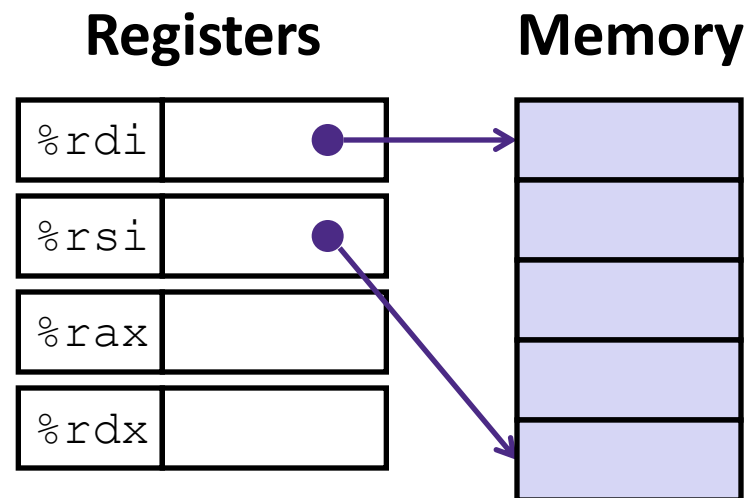
Compiler Explorer:

<https://godbolt.org/z/zc4Pcq>

# Understanding swap ()

```
void swap(long *xp, long *yp)
{
    long t0 = *xp;
    long t1 = *yp;
    *xp = t1;
    *yp = t0;
}
```

```
swap:
    movq    (%rdi), %rax
    movq    (%rsi), %rdx
    movq    %rdx, (%rdi)
    movq    %rax, (%rsi)
    ret
```



<u>Register</u>		<u>Variable</u>
%rdi	↔	xp
%rsi	↔	yp
%rax	↔	t0
%rdx	↔	t1

# Understanding swap ()

## Registers

%rdi	0x120
%rsi	0x100
%rax	
%rdx	

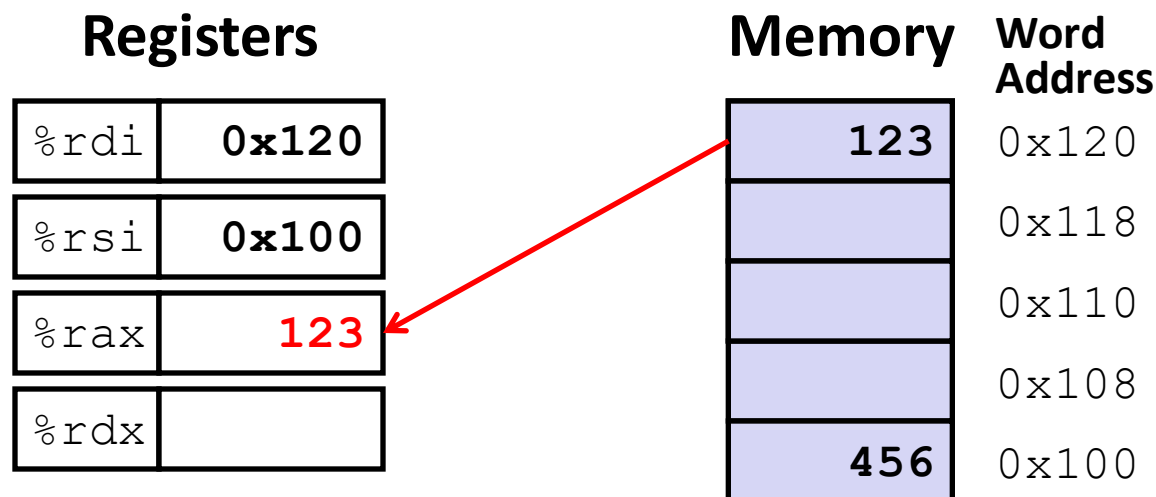
## Memory

	Word Address
123	0x120
	0x118
	0x110
	0x108
456	0x100

```
swap:
```

```
    movq    (%rdi), %rax    # t0 = *xp
    movq    (%rsi), %rdx    # t1 = *yp
    movq    %rdx, (%rdi)    # *xp = t1
    movq    %rax, (%rsi)    # *yp = t0
    ret
```

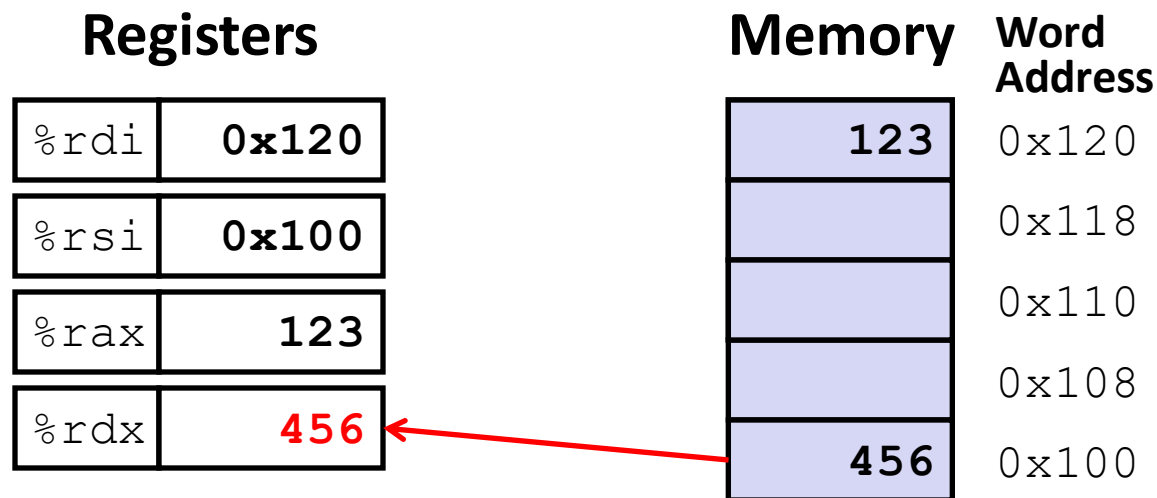
# Understanding swap ()



```
swap:
```

```
    movq    (%rdi), %rax    # t0 = *xp
    movq    (%rsi), %rdx    # t1 = *yp
    movq    %rdx, (%rdi)   # *xp = t1
    movq    %rax, (%rsi)   # *yp = t0
    ret
```

# Understanding swap ()

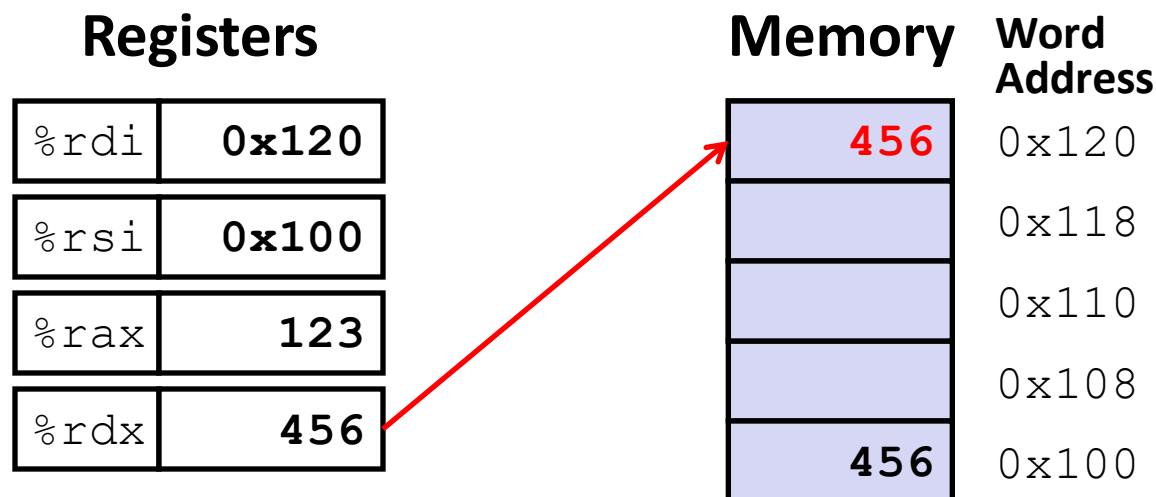


```
swap:
```

```
    movq    (%rdi), %rax    # t0 = *xp
    movq    (%rsi), %rdx    # t1 = *yp
    movq    %rdx, (%rdi)    # *xp = t1
    movq    %rax, (%rsi)    # *yp = t0
    ret
```



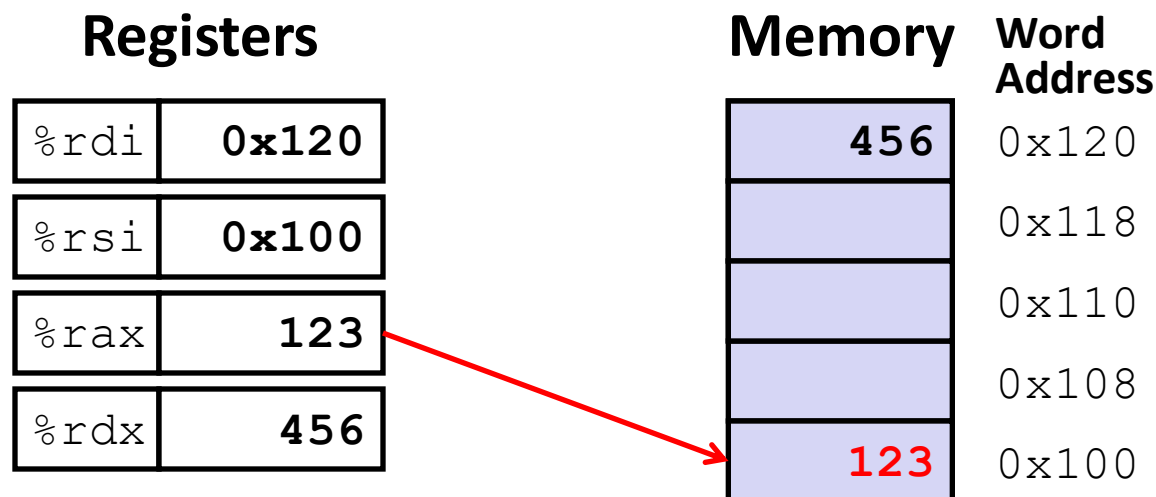
# Understanding swap ()



```
swap:
```

```
    movq    (%rdi), %rax    # t0 = *xp
    movq    (%rsi), %rdx    # t1 = *yp
    movq    %rdx, (%rdi)    # *xp = t1
    movq    %rax, (%rsi)    # *yp = t0
    ret
```

# Understanding swap ()



```
swap:
```

```
    movq    (%rdi), %rax    # t0 = *xp
    movq    (%rsi), %rdx    # t1 = *yp
    movq    %rdx, (%rdi)   # *xp = t1
    movq    %rax, (%rsi)   # *yp = t0
    ret
```

# Memory Addressing Modes: Basic

❖ **Indirect:**  $(R)$   $\text{Mem}[\text{Reg}[R]]$

- Data in register  $R$  specifies the memory address
- Like pointer dereference in C
- Example: `movq (%rcx), %rax`

❖ **Displacement:**  $D (R)$   $\text{Mem}[\text{Reg}[R]+D]$

- Data in register  $R$  specifies the *start* of some memory region
- Constant displacement  $D$  specifies the offset from that address
- Example: `movq 8(%rbp), %rdx`

# Complete Memory Addressing Modes

## ❖ General:

- $D(Rb, Ri, S) \quad \text{Mem}[\text{Reg}[Rb] + \text{Reg}[Ri] * S + D]$ 
  - Rb: Base register (any register)
  - Ri: Index register (any register except `%rsp`)
  - S: Scale factor (1, 2, 4, 8) – *why these numbers?*
  - D: Constant displacement value (a.k.a. immediate)

## ❖ Special cases (see CSPP Figure 3.3 on p.181)

- $D(Rb, Ri) \quad \text{Mem}[\text{Reg}[Rb] + \text{Reg}[Ri] + D] \quad (S=1)$
- $(Rb, Ri, S) \quad \text{Mem}[\text{Reg}[Rb] + \text{Reg}[Ri] * S] \quad (D=0)$
- $(Rb, Ri) \quad \text{Mem}[\text{Reg}[Rb] + \text{Reg}[Ri]] \quad (S=1, D=0)$
- $(, Ri, S) \quad \text{Mem}[\text{Reg}[Ri] * S] \quad (Rb=0, D=0)$

# Address Computation Examples

<code>%rdx</code>	<code>0xf000</code>
<code>%rcx</code>	<code>0x0100</code>

$D(Rb, Ri, S) \rightarrow$

$\text{Mem}[\text{Reg}[Rb] + \text{Reg}[Ri] * S + D]$

↑ ignore the memory access for now

Expression	Address Computation	Address (8 bytes wide)
<code>0x8 (%rdx)</code>		
<code>(%rdx, %rcx)</code>		
<code>(%rdx, %rcx, 4)</code>		
<code>0x80(, %rdx, 2)</code>		

# Reading Review

- ❖ Terminology:
  - Address Computation Instruction (`lea`)
  - Condition codes: Carry Flag (CF), Zero Flag (ZF), Sign Flag (SF), and Overflow Flag (OF)
  - Test (`test`) and compare (`cmp`) assembly instructions
  - Jump (`j*`) and set (`set*`) families of assembly instructions

# Review Questions

- ❖ Which of the following x86-64 instructions correctly calculates:  $\%rax = 9 * \%rdi$ 
  - A. `leaq (,%rdi,9), %rax`
  - B. `movq (,%rdi,9), %rax`
  - C. `leaq (%rdi,%rdi,8), %rax`
  - D. `movq (%rdi,%rdi,8), %rax`
- ❖ If  $\%rsi$  is `0x B0BACAFE 1EE7 F0 0D`, what is its value after executing `movswl %si, %esi`?

# Address Computation Instruction

- ❖ `leaq src, dst`
  - "lea" stands for *load effective address*
  - `src` is address expression (any of the formats we've seen)
  - `dst` is a register
  - Sets `dst` to the *address* computed by the `src` expression (**does not go to memory! – it just does math**)
  - Example: `leaq (%rdx, %rcx, 4), %rax`
- ❖ Uses:
  - Computing addresses without a memory reference
    - e.g. translation of `p = &x[i];`
  - Computing arithmetic expressions of the form  $x+k*i+d$ 
    - Though `k` can only be 1, 2, 4, or 8



# Example: lea vs. mov

## Registers

%rax	
%rbx	
%rcx	0x4
%rdx	0x100
%rdi	
%rsi	

## Memory Word Address

0x400	0x120
0xF	0x118
0x8	0x110
0x10	0x108
0x1	0x100

```
leaq (%rdx, %rcx, 4), %rax
movq (%rdx, %rcx, 4), %rbx
leaq (%rdx), %rdi
movq (%rdx), %rsi
```

lea – “It just does math”

# Arithmetic Example

```

long arith(long x, long y, long z)
{
    long t1 = x + y;
    long t2 = z + t1;
    long t3 = x + 4;
    long t4 = y * 48;
    long t5 = t3 + t4;
    long rval = t2 * t5;
    return rval;
}

```

```

arith:
    leaq    (%rdi,%rsi), %rax
    addq    %rdx, %rax
    leaq    (%rsi,%rsi,2), %rdx
    salq    $4, %rdx
    leaq    4(%rdi,%rdx), %rcx
    imulq   %rcx, %rax
    ret

```

Register	Use(s)
%rdi	1 <sup>st</sup> argument (x)
%rsi	2 <sup>nd</sup> argument (y)
%rdx	3 <sup>rd</sup> argument (z)

- ❖ Interesting Instructions
  - leaq: “address” computation
  - salq: shift
  - imulq: multiplication
    - Only used once!

# Arithmetic Example

```

long arith(long x, long y, long z)
{
    long t1 = x + y;
    long t2 = z + t1;
    long t3 = x + 4;
    long t4 = y * 48;
    long t5 = t3 + t4;
    long rval = t2 * t5;
    return rval;
}

```

Register	Use(s)
%rdi	x
%rsi	y
%rdx	z, t4
%rax	t1, t2, rval
%rcx	t5

```

arith:
    leaq    (%rdi,%rsi), %rax    # rax/t1    = x + y
    addq   %rdx, %rax          # rax/t2    = t1 + z
    leaq   (%rsi,%rsi,2), %rdx  # rdx       = 3 * y
    salq   $4, %rdx           # rdx/t4    = (3*y) * 16
    leaq   4(%rdi,%rdx), %rcx   # rcx/t5    = x + t4 + 4
    imulq  %rcx, %rax          # rax/rval  = t5 * t2
    ret

```

# Control Flow

Register	Use(s)
%rdi	1 <sup>st</sup> argument (x)
%rsi	2 <sup>nd</sup> argument (y)
%rax	return value

```
long max(long x, long y)
{
    long max;
    if (x > y) {
        max = x;
    } else {
        max = y;
    }
    return max;
}
```

```
max:
    ???
    movq    %rdi, %rax
    ???
    ???
    movq    %rsi, %rax
    ???
    ret
```

# Control Flow

Register	Use(s)
%rdi	1 <sup>st</sup> argument (x)
%rsi	2 <sup>nd</sup> argument (y)
%rax	return value

```
long max(long x, long y)
{
    long max;
    if (x > y) {
        max = x;
    } else {
        max = y;
    }
    return max;
}
```

**Conditional jump**

**Unconditional jump**

```
max:
    if x <= y then jump to else
    movq    %rdi, %rax
    jump to done
else:
    movq    %rsi, %rax
done:
    ret
```

# Conditionals and Control Flow

- ❖ Conditional branch/*jump*
  - Jump to somewhere else if some *condition* is true, otherwise execute next instruction
- ❖ Unconditional branch/*jump*
  - *Always* jump when you get to this instruction
- ❖ Together, they can implement most control flow constructs in high-level languages:
  - **if** (*condition*) **then** {...} **else** {...}
  - **while** (*condition*) {...}
  - **do** {...} **while** (*condition*)
  - **for** (*initialization*; *condition*; *iterative*) {...}
  - **switch** {...}

# Summary

- ❖ **Memory Addressing Modes:** The addresses used for accessing memory in `MOV` (and other) instructions can be computed in several different ways
  - *Base register, index register, scale factor, and displacement* map well to pointer arithmetic operations
- ❖ Control flow in x86 determined by Condition Codes