

x86-64 Programming II

CSE 351 Summer 2020

Instructor:

Porter Jones

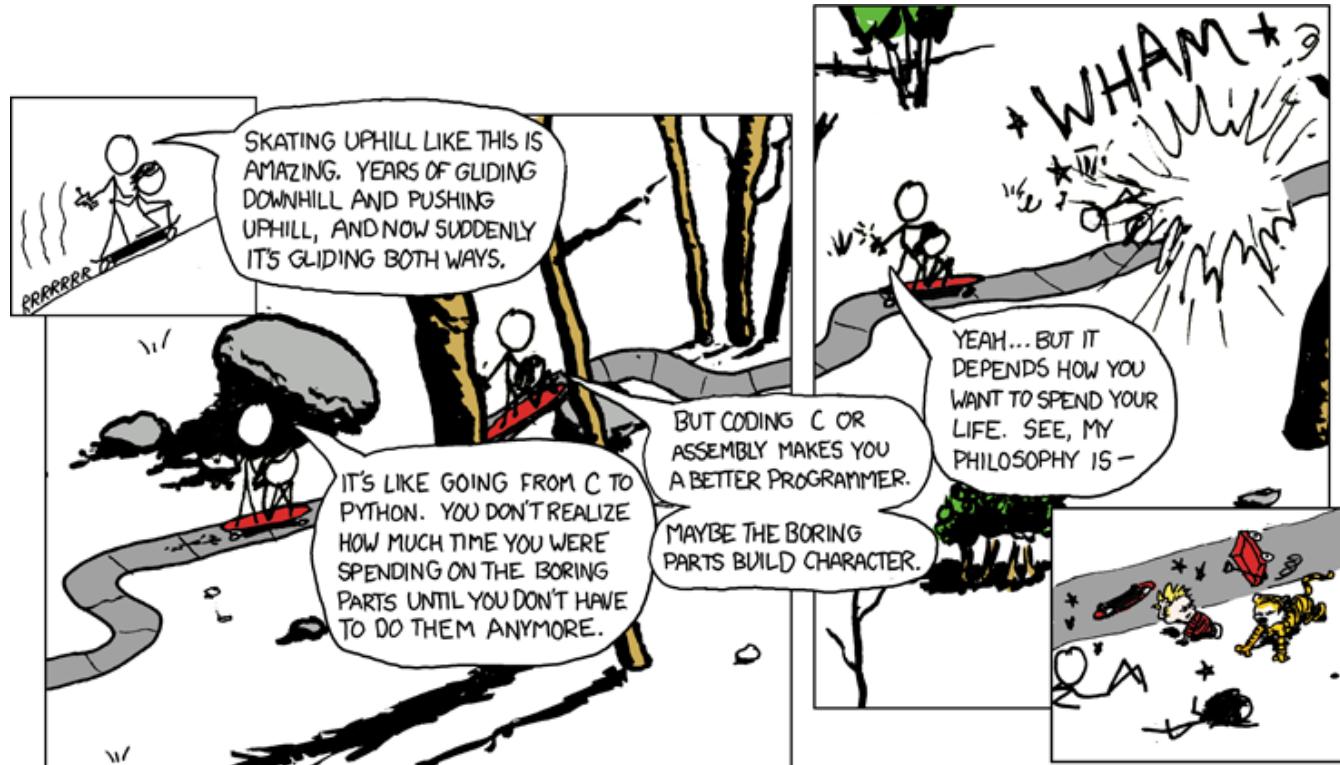
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<http://xkcd.com/409/>

Administrivia

- ❖ Questions doc: <https://tinyurl.com/CSE351-7-10>
- ❖ **See my email about accommodations!**
- ❖ Lab 1b now due Monday at 11:59pm (7/13)
 - Submit aisle_manager.c, store_client.c, and lab1Breflect.txt
 - Can still use late days until 7/15
- ❖ hw6, hw7 now due Monday (7/13) – 10:30am
- ❖ Unit Summary 1 now due Friday (7/17) – 11:59pm
 - Can still use late days until 7/20
- ❖ Mid-quarter Survey still due Friday (7/17) – 11:59pm
- ❖ hw8, hw9, hw10 now due Monday (7/20) – 10:30am

Administrivia

- ❖ Lab1a grades released later today
 - Talk to us about any questions you have!
 - Regrades open 24 hours after an assignment is due, stay open usually for about a week
- ❖ Lab 2 released later today!
 - Debugging x86-64 assembly using gdb
- ❖ I will now drop your lowest homework score (see Syllabus for more details).
 - Essentially will bump your homework total up by 11.5 points (the largest single homework total).

x86-64 Introduction

- ❖ Data transfer instruction (`mov`)
- ❖ Arithmetic operations
- ❖ **Memory addressing modes**
- ❖ **Address computation instruction (`lea`)**

Memory Addressing Modes: Basic

❖ Indirect: (R) $\text{Mem}[R]$

- Data in register R specifies the memory address
- Like pointer dereference in C
- Example: $\text{movq} (\%rcx), \%rax$
Copy 8-byte value from memory at & address
stored in %rcx to %rax

❖ Displacement: $D(R)$ $\text{Mem}[R+D]$

- Data in register R specifies the *start* of some memory region
- Constant displacement D specifies the offset from that address *n bytes*
- Example: $\text{movq} 8(\%rbp), \%rdx$

copy 8 byte value from memory at
address 8 bytes higher than address in %rbp
to %rdx

Complete Memory Addressing Modes

$$ar[i] = * (ar + i) = * (ar + j * \text{size of (type)})$$

any extra displacement

❖ General:

- $D(Rb, Ri, S)$ $\text{Mem}[\text{Reg}[Rb] + \text{Reg}[Ri] * S + D]$
 - Rb: Base register (any register)
 - Ri: Index register (any register except %rsp)
 - S: Scale factor (1, 2, 4, 8) – *why these numbers?* sizes of types!
 - D: Constant displacement value (a.k.a. immediate)

❖ Special cases (see CSPP Figure 3.3 on p.181)

- $D(Rb, Ri)$ $\text{Mem}[\text{Reg}[Rb] + \text{Reg}[Ri] + D]$ ($S=1$)
- (Rb, Ri, S) $\text{Mem}[\text{Reg}[Rb] + \text{Reg}[Ri] * S]$ ($D=0$)
- (Rb, Ri) $\text{Mem}[\text{Reg}[Rb] + \text{Reg}[Ri]]$ ($S=1, D=0$)
- $(, Ri, S)$ $\text{Mem}[\text{Reg}[Ri] * S]$ ($Rb=0, D=0$)

Address Computation Examples

%rdx	0xf000
%rcx	0x0100

$D(Rb, Ri, S) \rightarrow$
 $\text{Mem}[\text{Reg}[Rb] + \text{Reg}[Ri] * S + D]$

Expression	Address Computation	Address
$0x8(%rdx)$	$0xf000 + 0x8 =$	$0xf008$
$(%rdx, %rcx)$	$0xf000 + 0x100 =$	$0xf100$
$(%rdx, %rcx, 4)$	$0xf000 + 0x100 * 4 =$	$0x8400$
$0x80(,%rdx,2)$	$0xf000 * 2 + 0x80 =$	

Shifting trick $\rightarrow 0xf000 \ll 1 = 0x1e000$
 $0b\underline{1111}\underline{0000}\underline{0000}\underline{0000} \ll 1 = 0b\underline{1110}\underline{0000}\underline{0000}\underline{0000}$

Address Computation Instruction

- ❖ `leaq src, dst`
 - "lea" stands for *load effective address*
 - `src` is address expression (any of the formats we've seen)
 - `dst` is a register
 - Sets `dst` to the *address* computed by the `src` expression
(does not go to memory! – it just does math)
 - Example: `leaq (%rdx,%rcx,4), %rax`
$$\text{rax} = \underline{\text{rdx} + \text{rcx}*4}$$
no dereference
- ❖ Uses:
 - Computing addresses without a memory reference *these are slow*
 - e.g. translation of `p = &x[i];`
 - Computing arithmetic expressions of the form $x+k*i+d$
can do this fast!
 - Though `k` can only be 1, 2, 4, or 8

Example: lea vs. mov

Registers

%rax	0x110
%rbx	0x8
%rcx	0x4
%rdx	0x100
%rdi	0x100
%rsi	0x1

Memory

0x400
0xF
0x8
0x10
0x108

Word Address

0x120

0x118

0x110

0x108

0x100

$$\begin{aligned}(\text{rdx}, \text{rcx}, 2) &= \text{rdx} + \text{rcx} * 4 \\ &= 0x100 + 4 * 4 \\ &= 0x110\end{aligned}$$

no dereference

dereference occurs

```
leaq (%rdx,%rcx,4), %rax
movq (%rdx,%rcx,4), %rbx
leaq (%rdx), %rdi
movq (%rdx), %rsi
```

lea – “It just does math”

Arithmetic Example

```
long arith(long x, long y, long z)
{
    long t1 = x + y;
    long t2 = z + t1;
    long t3 = x + 4;
    long t4 = y * 48;
    long t5 = t3 + t4;
    long rval = t2 * t5;
    return rval;
}
```

Register	Use(s)
%rdi	1 st argument (x)
%rsi	2 nd argument (y)
%rdx	3 rd argument (z)

arith:

```
leaq    (%rdi,%rsi), %rax
addq    %rdx, %rax
leaq    (%rsi,%rsi,2), %rdx
salq    $4, %rdx
leaq    4(%rdi,%rdx), %rcx
imulq   %rcx, %rax
ret
```

- ❖ Interesting Instructions
 - leaq: “address” computation
 - salq: shift
 - imulq: multiplication
 - Only used once!

Arithmetic Example

```
long arith(long x, long y, long z)
{
    long t1 = x + y;
    long t2 = z + t1;
    long t3 = x + 4;
    long t4 = y * 48;
    long t5 = t3 + t4;
    long rval = t2 * t5;
    return rval;
}
```

Register	Use(s)
%rdi	x
%rsi	y
%rdx	z, t4
%rax	t1, t2, rval
%rcx	t5

$$\begin{aligned}
 &(\text{r21}, \text{rsi}) = \text{rdi} + \text{rsi} = x + y \\
 &(\text{rsi}, \text{rsi}, 2) = \text{rsi} + \text{rsi} * 2 = \text{rsi} * 3 \\
 &\qquad\qquad\qquad = y * 3
 \end{aligned}$$

arith:

leaq	(%rdi,%rsi), %rax	# rax/t1	= x + y
addq	%rdx, %rax	# rax/t2	= t1 + z
leaq	(%rsi,%rsi,2), %rdx	# rdx	= 3 * y
salq	\$4, %rdx	# rdx/t4	= (3*y) * 16
leaq	4(%rdi,%rdx), %rcx	# rcx/t5	= x + t4 + 4
imulq	%rcx, %rax	# rax/rval	= t5 * t2
ret			

Polling Question [Asm II – a]

- ❖ Which of the following x86-64 instructions correctly calculates $\%rax = 9 * \%rdi$?
 - Vote at <http://pollev.com/pbjones>

- A. ~~leaq (,%rdi,9), %rax~~ *must be 1, 2, 4, 8*
- B. ~~movq (,%rdi,9), %rax~~
- C. **leaq (%rdi,%rdi,8), %rax** $\Rightarrow rax = 9 * rdi$
- D. ~~movq (%rdi,%rdi,8), %rax~~ $\Rightarrow rax = 1 * (9 * rdi)$
- E. We're lost...

a move has
a dereference which
we don't want

Control Flow

```
long max(long x, long y)
{
    long max;
    if (x > y) {
        max = x;
    } else {
        max = y;
    }
    return max;
}
```

Register	Use(s)
%rdi	1 st argument (x)
%rsi	2 nd argument (y)
%rax	return value

```
max:
????
movq    %rdi, %rax
???
???
movq    %rsi, %rax
???
ret
```

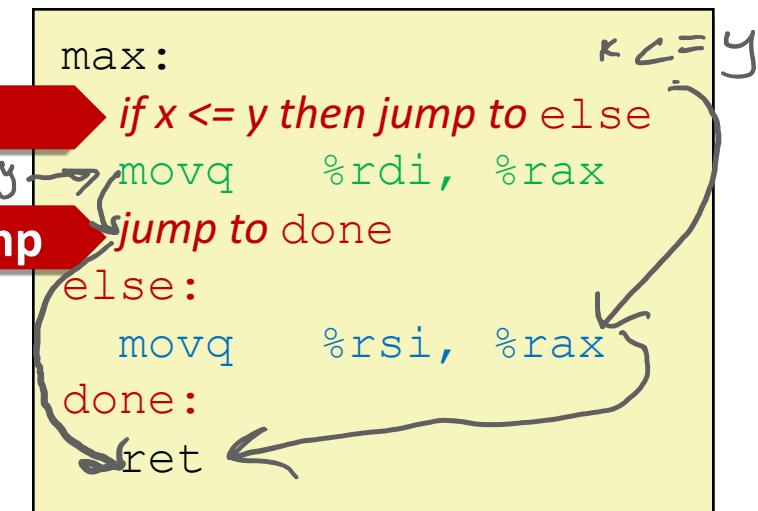
Control Flow

Register	Use(s)
%rdi	1 st argument (x)
%rsi	2 nd argument (y)
%rax	return value

```
long max(long x, long y)
{
    long max;
    if (x > y) {
        max = x;
    } else {
        max = y;
    }
    return max;
}
```

Conditional jump

Unconditional jump



Conditionals and Control Flow

- ❖ Conditional branch/*jump*
 - Jump to somewhere else if some *condition* is true, otherwise execute next instruction
- ❖ Unconditional branch/*jump*
 - Always jump when you get to this instruction
- ❖ Together, they can implement most control flow constructs in high-level languages:
 - **if** (*condition*) **then** { ... } **else** { ... }
 - **while** (*condition*) { ... }
 - **do** { ... } **while** (*condition*)
 - **for** (*initialization*; *condition*; *iterative*) { ... }
 - **switch** { ... }

x86 Control Flow

- ❖ Condition codes
- ❖ Conditional and unconditional branches
- ❖ Loops
- ❖ Switches

Processor State (x86-64, partial)

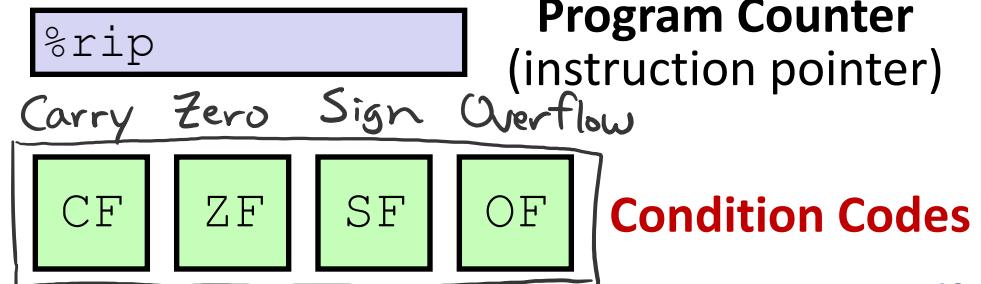
- ❖ Information about currently executing program
 - Temporary data (`%rax, ...`)
 - Location of runtime stack (`%rsp`)
 - Location of current code control point (`%rip, ...`)
 - Status of recent tests (**CF, ZF, SF, OF**) "flags"
 - Single bit registers:

Registers

<code>%rax</code>	<code>%r8</code>
<code>%rbx</code>	<code>%r9</code>
<code>%rcx</code>	<code>%r10</code>
<code>%rdx</code>	<code>%r11</code>
<code>%rsi</code>	<code>%r12</code>
<code>%rdi</code>	<code>%r13</code>
<code>%rsp</code>	<code>%r14</code>
<code>%rbp</code>	<code>%r15</code>



current top of the Stack



Condition Codes (Implicit Setting)

- ❖ *Implicitly set by arithmetic operations*

- (think of it as side effects)

- Example: **addq** src, dst $\leftrightarrow r = d+s$

- **CF=1** if carry out from MSB (*unsigned overflow*)

- **ZF=1** if $r==0$

- **SF=1** if $r<0$ (if MSB is 1)

- **OF=1** if *signed overflow*

$$(s>0 \quad \&\& \quad d>0 \quad \&\& \quad r<0) \quad || \quad (s<0 \quad \&\& \quad d<0 \quad \&\& \quad r>=0)$$

- **Not set by lea instruction (beware!)**

example:
~~rax = 0x800...00~~
~~addq %rax, %rax~~
~~Carry~~
~~0b100...000~~
~~+ 0b100...000~~
~~r = 0b000...000~~
~~CF = 1~~
~~ZF = 0~~
~~SF = 0~~
~~OF = 1~~
~~0 + 0 = 0 !~~



Condition Codes (Explicit Setting: Compare)

- ❖ *Explicitly set by Compare instruction*

- **cmpq** $\text{src1}, \text{src2}$ *like subq but doesn't store result*
- **cmpq** a, b sets flags based on $b-a$, but doesn't store $b-a$
 $r = b - a$
- **CF=1** if carry out from MSB (good for *unsigned* comparison)
- **ZF=1** if $a==b$ $(b-a \approx 0) \quad (r \approx 0)$
- **SF=1** if $(b-a) < 0$ (if MSB is 1) $(r < 0)$
- **OF=1** if *signed* overflow

$(a > 0 \quad \&\& \quad b < 0 \quad \&\& \quad (b-a) > 0) \quad ||$
 $(a < 0 \quad \&\& \quad b > 0 \quad \&\& \quad (b-a) < 0)$



Condition Codes (Explicit Setting: Test)

- ❖ *Explicitly set by Test instruction*

- **testq** src2, src1 *like and but doesn't store result*
- **testq** a, b sets flags based on a&b, but doesn't store a&b
 - Useful to have one of the operands be a *mask*

$$r = a \& b$$

$CF=0$

$OF=0$

- Can't have carry out (**CF**) or overflow (**OF**)
- **ZF=1** if $a \& b == 0$ ($r == 0$)
- **SF=1** if $a \& b < 0$ (signed) ($r < 0$)



Using Condition Codes: Jumping

❖ j* Instructions

- Jumps to **target** (an address) based on condition codes

don't worry about the details

result

(always compared to 0)

Instruction	Condition	Description (result always compared to 0)
<u>jmp</u> target	1	Unconditional
<u>je</u> target	ZF	Equal / Zero
<u>jne</u> target	~ZF	Not Equal / Not Zero
<u>js</u> target	SF	Negative
<u>jns</u> target	~SF	Nonnegative
<u>jg</u> target	~(SF^OF) & ~ZF	Greater (Signed)
<u>jge</u> target	~(SF^OF)	Greater or Equal (Signed)
<u>jl</u> target	(SF^OF)	Less (Signed)
<u>jle</u> target	(SF^OF) ZF	Less or Equal (Signed)
<u>ja</u> target	~CF & ~ZF	Above (unsigned ">")
<u>jb</u> target	CF	Below (unsigned "<")

Using Condition Codes: Setting

❖ set* Instructions

- Set low-order byte of dst to 0 or 1 based on condition codes
- Does not alter remaining 7 bytes

False = 0b 0000 0000 = 0x00
True = 0b 0000 0001 = 0x01

Instruction	Condition	Description
sete dst	ZF	Equal / Zero
setne dst	\sim ZF	Not Equal / Not Zero
sets dst	SF	Negative
setns dst	\sim SF	Nonnegative
setg dst	$\sim (SF \wedge OF) \ \& \ \sim ZF$	Greater (Signed)
setge dst	$\sim (SF \wedge OF)$	Greater or Equal (Signed)
setl dst	$(SF \wedge OF)$	Less (Signed)
setle dst	$(SF \wedge OF) \ \ ZF$	Less or Equal (Signed)
seta dst	$\sim CF \ \& \ \sim ZF$	Above (unsigned ">")
setb dst	CF	Below (unsigned "<")

Some
useful
as JX
Instructions

Reminder: x86-64 Integer Registers

- ❖ Accessing the low-order byte:

%rax	%al
------	-----

%rbx	%bl
------	-----

%rcx	%cl
------	-----

%rdx	%dl
------	-----

%rsi	%sil
------	------

%rdi	%dil
------	------

%rsp	%spl
------	------

%rbp	%bpl
------	------

%r8	%r8b
-----	------

%r9	%r9b
-----	------

%r10	%r10b
------	-------

%r11	%r11b
------	-------

%r12	%r12b
------	-------

%r13	%r13b
------	-------

%r14	%r14b
------	-------

%r15	%r15b
------	-------

↑
8B

↑
1B



Reading Condition Codes

e, ne, g, l, ...,

❖ set* Instructions

- Set a low-order byte to 0 or 1 based on condition codes
- Operand is byte register (e.g. al, dl) or a byte in memory
- Do not alter remaining bytes in register
 - Typically use movzbl (zero-extended mov) to finish job

```
int gt(long x, long y)
{
    return x > y;
}
```

Register	Use(s)
%rdi	1 st argument (x)
%rsi	2 nd argument (y)
%rax	return value

```
cmpq    %rsi, %rdi    #
setg    %al           #
movzbl  %al, %eax   #
ret
```

Reading Condition Codes

❖ set* Instructions

- Set a low-order byte to 0 or 1 based on condition codes
- Operand is byte register (e.g. al, dl) or a byte in memory
- Do not alter remaining bytes in register
 - Typically use movzbl (zero-extended mov) to finish job

```
int gt(long x, long y)
{
    return x > y;
}
```

```
cmpq %rsi, %rdi      # Compare x:y
setg %al              # Set when >
movzbl %al, %eax     # Zero rest of %rax
ret
```

Register	Use(s)
%rdi	1 st argument (x)
%rsi	2 nd argument (y)
%rax	return value

*cmpq %rsi, %rdi $\Rightarrow r = rdi - rsi$
 $= x - y$*

*setg %al \Rightarrow Set %al to 1 if
 $x - y > 0$
 $x > y$*

f.all remaining
bytes w/zeros
of sat

Aside: `movz` and `movs`

src width → *dest width*

```
movz _____ src, regDest
movs _____ src, regDest
```

2 width
specifiers
(b, w, l, q)

Move with zero extension
Move with sign extension

- Copy from a *smaller* source value to a *larger* destination
- Source can be memory or register; Destination *must* be a register
- Fill remaining bits of dest with **zero** (`movz`) or **sign bit** (`movs`)

`movzSD` / `movsSD`:

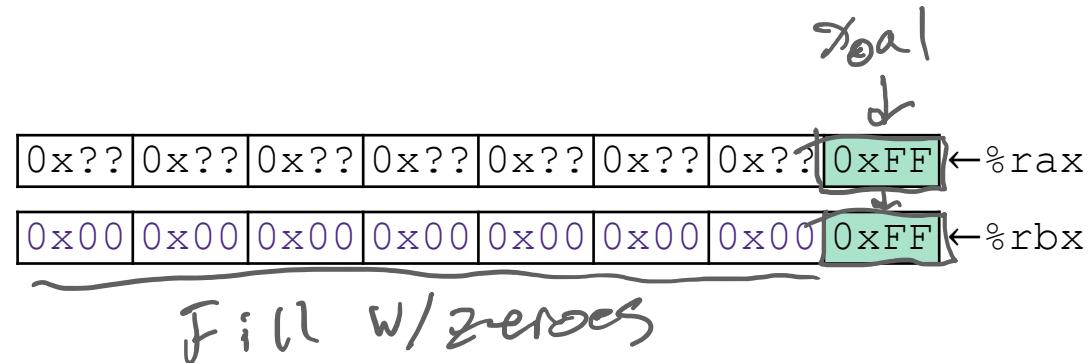
S – size of source (**b** = 1 byte, **w** = 2)

D – size of dest (**w** = 2 bytes, **l** = 4, **q** = 8)

Example:

fill w/ 0s → *8 bytes*

`movzbq %al, %rbx`



Aside: `movz` and `movs`

`movz __ src, regDest` # Move with zero extension

`movs __ src, regDest` # Move with sign extension

- Copy from a *smaller* source value to a *larger* destination
- Source can be memory or register; Destination *must* be a register
- Fill remaining bits of dest with **zero** (`movz`) or **sign bit** (`movs`)

`movz SD` / `movs SD`:

S – size of source (**b** = 1 byte, **w** = 2)

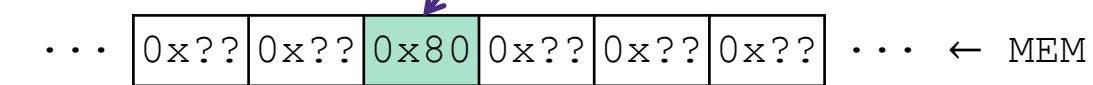
D – size of dest (**w** = 2 bytes, **l** = 4, **q** = 8)

Example:

`movsb1 (%rax), %ebx`

Copy 1 byte from memory into
8-byte register & sign extend it

Note: In x86-64, any instruction that generates a 32-bit (long word) value for a register also sets the high-order portion of the register to 0. Good example on p. 184 in the textbook.



Summary

- ❖ **Memory Addressing Modes:** The addresses used for accessing memory in `mov` (and other) instructions can be computed in several different ways
 - *Base register, index register, scale factor, and displacement* map well to pointer arithmetic operations
- ❖ Control flow in x86 determined by status of Condition Codes
 - Showed Carry, Zero, Sign, and Overflow, though others exist
 - Set flags with arithmetic instructions (implicit) or Compare and Test (explicit)
 - Set instructions read out flag values
 - Jump instructions use flag values to determine next instruction to execute