Virtual Memory III
CSE 351 Spring 2020

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https://xkcd.com/2308/
Adminstrivia

- Lab 4 – Due Friday 5/22
  - Cache parameter puzzles and code optimizations

- You must log on with your @uw google account to access!!
  - Google doc for 11:30 Lecture: [https://tinyurl.com/351-05-20A](https://tinyurl.com/351-05-20A)
Address Translation: Page Hit

1) Processor sends virtual address to MMU (memory management unit)

2-3) MMU fetches PTE from page table in cache/memory
    (Uses PTBR to find beginning of page table for current process)

4) MMU sends physical address to cache/memory requesting data

5) Cache/memory sends data to processor

VA = Virtual Address  PTEA = Page Table Entry Address  PTE= Page Table Entry
PA = Physical Address  Data = Contents of memory stored at VA originally requested by CPU
Address Translation: Page Fault

1) Processor sends virtual address to MMU
2-3) MMU fetches PTE from page table in cache/memory
4) Valid bit is zero, so MMU triggers page fault exception
5) Handler identifies victim (and, if dirty, pages it out to disk)
6) Handler pages in new page and updates PTE in memory
7) Handler returns to original process, restarting faulting instruction
Hmm... Translation Sounds Slow

- The MMU accesses memory *twice*: once to get the PTE for translation, and then again for the actual memory request
  - The PTEs *may* be cached in L1 like any other memory word
    - But they may be evicted by other data references
    - And a hit in the L1 cache still requires 1-3 cycles

- *What can we do to make this faster?*
  - **Solution:** add another cache! 🎉
Speeding up Translation with a TLB

Translation Lookaside Buffer (TLB):

- Small hardware cache in MMU
  - Split VPN into TLB Tag and TLB Index based on # of sets in TLB
- Maps virtual page numbers to physical page numbers
- Stores page table entries for a small number of pages
  - Modern Intel processors have 128 or 256 entries in TLB
- Much faster than a page table lookup in cache/memory

![Diagram of TLB]
A TLB hit eliminates a memory access!
A TLB miss incurs an additional memory access (the PTE)

- Fortunately, TLB misses are rare
Fetching Data on a Memory Read

1) Check TLB
   - **Input**: VPN, **Output**: PPN
   - **TLB Hit**: Fetch translation, return PPN
   - **TLB Miss**: Check page table (in memory)
     - **Page Table Hit**: Load page table entry into TLB
     - **Page Fault**: Fetch page from disk to memory, update corresponding page table entry, then load entry into TLB

2) Check cache
   - **Input**: physical address, **Output**: data
   - **Cache Hit**: Return data value to processor
   - **Cache Miss**: Fetch data value from memory, store it in cache, return it to processor
Address Translation

Virtual Address

TLB Lookup

TLB Miss

Check the Page Table

TLB Hit

Protection Check

Page not in Mem

Page Fault (OS loads page)

Access Denied

SIGSEGV

Page in Mem

Update TLB

Access Permitted

Find in Mem

Find in Disk

Physical Address

Page in Mem

Protection Fault

Check cache

Miss

Hit
Address Manipulation

request from CPU: $n$-bit virtual address

split to access TLB: TLB Tag, TLB Index, Page Offset

(on TLB miss) access PT: Virtual Page Number, Page offset

$m$-bit physical address: Physical Page Number, Page offset

split to access cache: Cache Tag, Cache Index, Offset
Context Switching Revisited

What needs to happen when the CPU switches processes?

- Registers:
  - Save state of old process, load state of new process
  - Including the Page Table Base Register (PTBR)

- Memory:
  - Nothing to do! Pages for processes already exist in memory/disk and protected from each other

- TLB:
  - *Invalidate* all entries in TLB – mapping is for old process’ VAs

- Cache:
  - Can leave alone because storing based on PAs – good for shared data
Summary of Address Translation Symbols

- **Basic Parameters**
  - $N = 2^n$ Number of addresses in virtual address space
  - $M = 2^m$ Number of addresses in physical address space
  - $P = 2^p$ Page size (bytes)

- **Components of the virtual address (VA)**
  - VPO Virtual page offset
  - VPN Virtual page number
  - TLBI TLB index
  - TLBT TLB tag

- **Components of the physical address (PA)**
  - PPO Physical page offset (same as VPO)
  - PPN Physical page number
Simple Memory System Example (small)

- **Addressing**
  - 14-bit virtual addresses
  - 12-bit physical address
  - Page size = 64 bytes
Simple Memory System: Page Table

- Only showing first 16 entries (out of ____)
  - **Note:** showing 2 hex digits for PPN even though only 6 bits
  - **Note:** other management bits not shown, but part of PTE

<table>
<thead>
<tr>
<th>VPN</th>
<th>PPN</th>
<th>Valid</th>
</tr>
</thead>
<tbody>
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<td>1</td>
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</tr>
<tr>
<td>F</td>
<td>0D</td>
<td>1</td>
</tr>
</tbody>
</table>
## Simple Memory System: TLB

- **16 entries total**
- **4-way set associative**

### TLB Index and Tag

<table>
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<tr>
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<th>Tag</th>
<th>PPN</th>
<th>Valid</th>
<th>Tag</th>
<th>PPN</th>
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<td></td>
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<td>34</td>
<td>1</td>
<td>02</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Why does the TLB ignore the page offset?
Simple Memory System: Cache

- Direct-mapped with $K = 4$ B, $C/K = 16$
- Physically addressed

### Direct-Mapped Cache

<table>
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<tr>
<th>Index</th>
<th>Tag</th>
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<th>B3</th>
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<tbody>
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<td></td>
</tr>
<tr>
<td>2</td>
<td>1B</td>
<td>1</td>
<td>00</td>
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### Physically Addressed Cache

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</tbody>
</table>

**Note:** It is just coincidence that the PPN is the same width as the cache tag
# Current State of Memory System

## TLB:

<table>
<thead>
<tr>
<th>Set</th>
<th>Tag</th>
<th>PPN</th>
<th>V</th>
<th>Tag</th>
<th>PPN</th>
<th>V</th>
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</table>

## Page table (partial):

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## Cache:

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</table>
Polling Question [VM III]
Memory Request Example #1

- **Virtual Address:** 0x03D4

  - **TLBT:** 0000111110100
  - **TLBI:** 0000111110100
  - **VPN:** 0000111110100
  - **VPO:**

  - **VPN:**
  - **TLBT:**
  - **TLBI:**
  - **TLB Hit?**
  - **Page Fault?**
  - **PPN:**

- **Physical Address:**

  - **CT:**
  - **Cl:**
  - **CO:**
  - **PPN:**
  - **PPO:**

  - **CT:**
  - **Cl:**
  - **CO:**
  - **Cache Hit?**
  - **Data (byte):**

**Note:** It is just coincidence that the PPN is the same width as the cache Tag.
Memory Request Example #2

- **Virtual Address**: \(0x038F\)

- **Physical Address**: 

---

**Note:** It is just coincidence that the PPN is the same width as the cache Tag.
Memory Request Example #3

- Virtual Address: \texttt{0x0020}

Note: It is just coincidence that the PPN is the same width as the cache Tag

- Physical Address:
Memory Request Example #4

- Virtual Address: \(0x036B\)

![Virtual Address Diagram]

- Physical Address:

![Physical Address Diagram]

Note: It is just coincidence that the PPN is the same width as the cache Tag.
Memory Overview

- `movl 0x8043ab, %rdi`

Diagram:
- CPU
- MMU
- TLB
- Cache
  - requested 32-bits
- Main memory (DRAM)
  - Page
  - Line
- Disk
- Page

Block
Page Table Reality

- Just one issue... the numbers don’t work out for the story so far!

- The problem is the page table for each process:
  - Suppose 64-bit VAs, 8 KiB pages, 8 GiB physical memory
  - How many page table entries is that?

  - About how long is each PTE?

- **Moral:** Cannot use this naïve implementation of the virtual→physical page mapping – it’s way too big
A Solution: Multi-level Page Tables

This is called a *page walk*

This is extra (non-testable) material
Multi-level Page Tables

- A tree of depth $k$ where each node at depth $i$ has up to $2^j$ children if part $i$ of the VPN has $j$ bits
- Hardware for multi-level page tables inherently more complicated
  - But it’s a necessary complexity – 1-level does not fit
- Why it works: Most subtrees are not used at all, so they are never created and definitely aren’t in physical memory
  - Parts created can be evicted from cache/memory when not being used
  - Each node can have a size of ~1-100KB
- But now for a $k$-level page table, a TLB miss requires $k + 1$ cache/memory accesses
  - Fine so long as TLB misses are rare – motivates larger TLBs
Practice VM Question

- Our system has the following properties
  - 1 MiB of physical address space
  - 4 GiB of virtual address space
  - 32 KiB page size
  - 4-entry fully associative TLB with LRU replacement

(a) Fill in the following blanks:

- ________ Entries in a page table
- ________ Minimum bit-width of PTBR
- ________ TLBT bits
- ________ Max # of valid entries in a page table
Practice VM Question

- One process uses a page-aligned *square* matrix `mat[]` of 32-bit integers in the code shown below:

  ```
  #define MAT_SIZE = 2048
  for(int i = 0; i < MAT_SIZE; i++)
      mat[i*(MAT_SIZE+1)] = i;
  ```

b) What is the largest stride (in bytes) between successive memory accesses (in the VA space)?
Practice VM Question

- One process uses a page-aligned square matrix `mat[]` of 32-bit integers in the code shown below:
  ```c
  #define MAT_SIZE = 2048
  for(int i = 0; i < MAT_SIZE; i++)
      mat[i*(MAT_SIZE+1)] = i;
  ```

- Assuming all of `mat[]` starts on disk, what are the following hit rates for the execution of the for-loop?
  - _________  TLB Hit Rate
  - _________  Page Table Hit Rate
Virtual Memory Summary

- **Programmer’s view of virtual memory**
  - Each process has its own private linear address space
  - Cannot be corrupted by other processes

- **System view of virtual memory**
  - Uses memory efficiently by caching virtual memory pages
    - Efficient only because of locality
  - Simplifies memory management and sharing
  - Simplifies protection by providing permissions checking
Memory System Summary

- Memory Caches (L1/L2/L3)
  - Purely a speed-up technique
  - Behavior invisible to application programmer and (mostly) OS
  - Implemented totally in hardware

- Virtual Memory
  - Supports many OS-related functions
    - Process creation, task switching, protection
  - Operating System (software)
    - Allocates/shares physical memory among processes
    - Maintains high-level tables tracking memory type, source, sharing
    - Handles exceptions, fills in hardware-defined mapping tables
  - Hardware
    - Translates virtual addresses via mapping tables, enforcing permissions
    - Accelerates mapping via translation cache (TLB)