x86-64 Programming I
CSE 351 Spring 2020

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Edan Sneh
Jonathan Chen
Jeffery Tian
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Joseph Schafer
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Eddy (Tianyi) Zhou

http://www.smbc-comics.com/?id=2999
Administrivia

- hw7 due Friday – 11am, hw8 due Monday – 11am
- Lab 1b due Monday (4/20)
  - Submit `bits.c` and `lab1Breflect.txt`

- You must log on with your @uw google account to access!!
  - Google doc for 11:30 Lecture: https://tinyurl.com/351-04-15A

- Week 2 Feedback Survey
  - https://catalyst.uw.edu/webq/survey/rea2000/388285
Roadmap

C:

```c
car *c = malloc(sizeof(car));
c->miles = 100;
c->gals = 17;
float mpg = get_mpg(c);
free(c);
```

Java:

```java
Car c = new Car();
c.setMiles(100);
c.setGals(17);
float mpg =
c.getMPG();
```

Assembly language:

```assembly
get_mpg:
    pushq %rbp
    movq %rsp, %rbp
    ...
    popq %rbp
    ret
```

Machine code:

```
0111010000011000
100011010000010000000010
1000100111000010
1100001111111101000011111
```

OS:

- Windows 10
- OS X Yosemite

Memory & data
Integers & floats
x86 assembly
Procedures & stacks
Executables
Arrays & structs
Memory & caches
Processes
Virtual memory
Memory allocation
Java vs. C
Architecture Sits at the Hardware Interface

**Source code**
Different applications or algorithms

**Compiler**
Perform optimizations, generate instructions

**Architecture**
Instruction set

**Hardware**
Different implementations

- Intel Pentium 4
- Intel Core 2
- Intel Core i7
- AMD Opteron
- AMD Athlon
- ARM Cortex-A53
- Apple A7

C Language

- Program A
- Program B
- Your program

Compiler

- GCC
- Clang

We will be using

**x86-64**

**ARMv8 (AArch64/A64)**
Definitions

- **Architecture (ISA):** The parts of a processor design that one needs to understand to write assembly code
  - “What is directly visible to software”

- **Microarchitecture:** Implementation of the architecture
  - CSE/EE 469
Instruction Set Architectures

- The ISA defines:
  - The system’s state (e.g. registers, memory, program counter)
  - The instructions the CPU can execute
  - The effect that each of these instructions will have on the system state
Instruction Set Philosophies

- **Complex Instruction Set Computing (CISC):** Add more and more elaborate and specialized instructions as needed
  - Lots of tools for programmers to use, but hardware must be able to handle all instructions
  - x86-64 is CISC, but only a small subset of instructions encountered with Linux programs

- **Reduced Instruction Set Computing (RISC):** Keep instruction set small and regular
  - Easier to build fast hardware
  - Let software do the complicated operations by composing simpler ones
General ISA Design Decisions

- Instructions
  - What instructions are available? What do they do?
  - How are they encoded?

- Registers
  - How many registers are there?
  - How wide are they?

- Memory
  - How do you specify a memory location?
### Mainstream ISAs

<table>
<thead>
<tr>
<th>Designer</th>
<th>Intel, AMD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits</td>
<td>16-bit, 32-bit and 64-bit</td>
</tr>
<tr>
<td>Introduced</td>
<td>1978 (16-bit), 1985 (32-bit), 2003 (64-bit)</td>
</tr>
<tr>
<td>Design</td>
<td>CISC</td>
</tr>
<tr>
<td>Type</td>
<td>Register-memory</td>
</tr>
<tr>
<td>Encoding</td>
<td>Variable (1 to 15 bytes)</td>
</tr>
<tr>
<td>Endianness</td>
<td>Little</td>
</tr>
</tbody>
</table>

#### x86
- Macbooks & PCs (Core i3, i5, i7, M)
- x86-64 Instruction Set

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#### ARM architectures

<table>
<thead>
<tr>
<th>Designer</th>
<th>ARM Holdings</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits</td>
<td>32-bit, 64-bit</td>
</tr>
<tr>
<td>Introduced</td>
<td>1985; 31 years ago</td>
</tr>
<tr>
<td>Design</td>
<td>RISC</td>
</tr>
<tr>
<td>Type</td>
<td>Register-Register</td>
</tr>
<tr>
<td>Encoding</td>
<td>AArch64/A64 and AArch32/A32 use 32-bit instructions, T32 (Thumb-2) uses mixed 16- and 32-bit instructions. ARMv7 user-space compatibility[1]</td>
</tr>
<tr>
<td>Endianness</td>
<td>Little</td>
</tr>
</tbody>
</table>

#### ARM Instruction Set

- Smartphone-like devices (iPhone, iPad, Raspberry Pi)

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#### MIPS

<table>
<thead>
<tr>
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<th>MIPS Technologies, Inc.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits</td>
<td>64-bit (32→64)</td>
</tr>
<tr>
<td>Introduced</td>
<td>1981; 35 years ago</td>
</tr>
<tr>
<td>Design</td>
<td>RISC</td>
</tr>
<tr>
<td>Type</td>
<td>Register-Register</td>
</tr>
<tr>
<td>Encoding</td>
<td>Fixed</td>
</tr>
<tr>
<td>Endianness</td>
<td>Bi</td>
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</tbody>
</table>

#### MIPS Instruction Set

- Digital home & networking equipment (Blu-ray, PlayStation 2)
Writing Assembly Code? In 2020???

- Chances are, you’ll never write a program in assembly, but understanding assembly is the key to the machine-level execution model:
  - Behavior of programs in the presence of bugs
    - When high-level language model breaks down
  - Tuning program performance
    - Understand optimizations done/not done by the compiler
    - Understanding sources of program inefficiency
  - Implementing systems software
    - What are the “states” of processes that the OS must manage
    - Using special units (timers, I/O co-processors, etc.) inside processor!
  - Fighting malicious software
    - Distributed software is in binary form
Assembly Programmer’s View

- **Programmer-visible state**
  - **PC**: the Program Counter (%rip in x86-64)
    - Address of next instruction
  - **Named registers**
    - Together in “register file”
    - Heavily used program data
  - **Condition codes**
    - Store status information about most recent arithmetic operation
    - Used for conditional branching

- **Memory**
  - Byte-addressable array
  - Code and user data
  - Includes the Stack (for supporting procedures)
x86-64 Assembly “Data Types”

- **Integral data of 1, 2, 4, or 8 bytes**
  - Data values
  - Addresses

- **Floating point data of 4, 8, 10 or 2x8 or 4x4 or 8x2**
  - Different registers for those (e.g. %xmm1, %ymm2)
  - Come from extensions to x86 (SSE, AVX, ...)

- **No aggregate types such as arrays or structures**
  - Just contiguously allocated bytes in memory

- **Two common syntaxes**
  - “AT&T”: used by our course, slides, textbook, gnu tools, ...
  - “Intel”: used by Intel documentation, Intel tools, ...
  - Must know which you’re reading
What is a Register?

- A location in the CPU that stores a small amount of data, which can be accessed very quickly (once every clock cycle)

- Registers have names, not addresses
  - In assembly, they start with $\%$ (e.g. $\%rsi$)

- Registers are at the heart of assembly programming
  - They are a precious commodity in all architectures, but especially x86 only 16 of them...
**x86-64 Integer Registers – 64 bits wide**

- **Can reference low-order 4 bytes (also low-order 2 & 1 bytes)**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
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<tbody>
<tr>
<td>%rax</td>
<td>%eax</td>
</tr>
<tr>
<td>%rbx</td>
<td>%ebx</td>
</tr>
<tr>
<td>%rcx</td>
<td>%ecx</td>
</tr>
<tr>
<td>%rdx</td>
<td>%edx</td>
</tr>
<tr>
<td>%rsi</td>
<td>%esi</td>
</tr>
<tr>
<td>%rdi</td>
<td>%edi</td>
</tr>
<tr>
<td>%rsp</td>
<td>%esp</td>
</tr>
<tr>
<td>%rbp</td>
<td>%ebp</td>
</tr>
</tbody>
</table>

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<tbody>
<tr>
<td>%r8</td>
<td>%r8d</td>
</tr>
<tr>
<td>%r9</td>
<td>%r9d</td>
</tr>
<tr>
<td>%r10</td>
<td>%r10d</td>
</tr>
<tr>
<td>%r11</td>
<td>%r11d</td>
</tr>
<tr>
<td>%r12</td>
<td>%r12d</td>
</tr>
<tr>
<td>%r13</td>
<td>%r13d</td>
</tr>
<tr>
<td>%r14</td>
<td>%r14d</td>
</tr>
<tr>
<td>%r15</td>
<td>%r15d</td>
</tr>
</tbody>
</table>
### Some History: IA32 Registers – 32 bits wide

#### General Purpose Registers:
- **eax**, **ax**, **ah**, **al**: 32 bits (same as last slide)
- **ecx**, **cx**, **ch**, **cl**: 16 bits
- **edx**, **dx**, **dh**, **dl**: 16 bits
- **ebx**, **bx**, **bh**, **bl**: 16 bits
- **esi**, **si**: 16 bits
- **edi**, **di**: 16 bits
- **esp**, **sp**: 16 bits
- **ebp**, **bp**: 16 bits

#### 8-bit Registers:
- **esi**, **si**: accumulate
- **edi**, **di**: counter
- **esp**, **sp**: data
- **ebp**, **bp**: base
- **esi**, **si**: source index
- **edi**, **di**: destination index

#### 16-bit Virtual Registers (backwards compatibility):
- **esi**, **si**: source index
- **edi**, **di**: destination index

#### Name Origin (mostly obsolete):
- **esi**, **si**: source index
- **edi**, **di**: destination index

#### Backwards Compatibility:
- **%esi**, **%si**: source index
- **%edi**, **%di**: destination index
- **%esp**, **%sp**: stack pointer
- **%ebp**, **%bp**: base pointer
Memory vs. Registers

- **Addresses**
  - 0x7FFFD024C3DC

- **Big**
  - ~8 GiB

- **Slow**
  - ~50-100 ns

- **Dynamic**
  - Can “grow” as needed while program runs

- **Names**
  - %rdi

- **Small**
  - (16 x 8 B) = 128 B

- **Fast**
  - sub-nanosecond timescale

- **Static**
  - fixed number in hardware
Three Basic Kinds of Instructions

1) **Transfer data between memory and register**
   - **Load** data from memory into register
     - \( \%\text{reg} = \text{Mem}[\text{address}] \)
   - **Store** register data into memory
     - \( \text{Mem}[\text{address}] = \%\text{reg} \)

2) **Perform arithmetic operation on register or memory data**
   - \( c = a + b; \quad z = x << y; \quad i = h \& g; \)

3) **Control flow:** what instruction to execute next
   - Unconditional jumps to/from procedures
   - Conditional branches
Operand types

- **Immediate**: Constant integer data
  - Examples: $0x400, $-533
  - Like C literal, but prefixed with `$`
  - Encoded with 1, 2, 4, or 8 bytes depending on the instruction

- **Register**: 1 of 16 integer registers
  - Examples: %rax, %r13
  - But %rsp reserved for special use
  - Others have special uses for particular instructions

- **Memory**: Consecutive bytes of memory at a computed address
  - Simplest example: (%rax)
  - Various other “address modes”
x86-64 Introduction

- Data transfer instruction (mov)
- Arithmetic operations
- Memory addressing modes
  - swap example
- Address computation instruction (lea)
Moving Data

- **General form:** `mov_ source, destination`
  - Missing letter (\_) specifies size of operands
  - Note that due to backwards-compatible support for 8086 programs (16-bit machines!), "word" means 16 bits = 2 bytes in x86 instruction names
  - Lots of these in typical code

- `movb src, dst`  
  - Move 1-byte "byte"

- `movw src, dst`  
  - Move 2-byte "word"

- `movl src, dst`  
  - Move 4-byte "long word"

- `movq src, dst`  
  - Move 8-byte "quad word"
Operand Combinations

<table>
<thead>
<tr>
<th>Source</th>
<th>Dest</th>
<th>Src, Dest</th>
<th>C Analog</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>movq $0x4, %rax</td>
<td>var_a = 0x4;</td>
</tr>
<tr>
<td></td>
<td></td>
<td>movq $-147, (%rax)</td>
<td>*p_a = -147;</td>
</tr>
<tr>
<td>movq</td>
<td>Reg</td>
<td>movq %rax, %rdx</td>
<td>var_d = var_a;</td>
</tr>
<tr>
<td></td>
<td>Mem</td>
<td>movq %rax, (%rdx)</td>
<td>*p_d = var_a;</td>
</tr>
<tr>
<td></td>
<td>Mem</td>
<td>movq (%rax), %rdx</td>
<td>var_d = *p_a;</td>
</tr>
</tbody>
</table>

- Cannot do memory-memory transfer with a single instruction
  - How would you do it?
    1. Mem → Reg
    2. Reg → Mem
Some Arithmetic Operations

- Binary (two-operand) Instructions:
  - Maximum of one memory operand
  - Beware argument order!
  - No distinction between signed and unsigned
    - Only arithmetic vs. logical shifts
  - How do you implement \( r3 = r1 + r2 \)?

<table>
<thead>
<tr>
<th>Format</th>
<th>Computation</th>
</tr>
</thead>
<tbody>
<tr>
<td>addq src, dst</td>
<td>( dst = dst + src )</td>
</tr>
<tr>
<td>subq src, dst</td>
<td>( dst = dst - src )</td>
</tr>
<tr>
<td>imulq src, dst</td>
<td>( dst = dst * src )</td>
</tr>
<tr>
<td>sarq src, dst</td>
<td>( dst = dst &gt;&gt; src )</td>
</tr>
<tr>
<td>shrq src, dst</td>
<td>( dst = dst &gt;&gt; src )</td>
</tr>
<tr>
<td>shlq src, dst</td>
<td>( dst = dst &lt;&lt; src )</td>
</tr>
<tr>
<td>xorq src, dst</td>
<td>( dst = dst ^ src )</td>
</tr>
<tr>
<td>andq src, dst</td>
<td>( dst = dst &amp; src )</td>
</tr>
<tr>
<td>orq src, dst</td>
<td>( dst = dst</td>
</tr>
</tbody>
</table>

Other ways to set to 0:
- \( \text{subq} \%rcx, \%rcx \)
- \( \text{andq} \$0, \%rcx \)
- \( \text{xorq} \%rnx, \%rcx \)
- \( \text{imulq} \$0, \%rcx \)
Polling Question [Asm I – a]

- Assume: r3 is in %rcx, r1 is in %rax, and r2 is in %rbx
  which of the following would implement:
  \[ r3 = r1 + r2 \]

- Vote at http://pollev.com/rea

A. `addq %rax, %rbx, %rcx`
B. `addq %rcx, %rax, %rbx`
C. `movq %rax, %rcx
  addq %rbx, %rcx`
D. `movq (%rbx), %rcx
  addq (%rax), %rcx`
E. We’re lost...
Some Arithmetic Operations

- Unary (one-operand) Instructions:

<table>
<thead>
<tr>
<th>Format</th>
<th>Computation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>incq</td>
<td>dst = dst + 1</td>
<td>increment</td>
</tr>
<tr>
<td>decq</td>
<td>dst = dst - 1</td>
<td>decrement</td>
</tr>
<tr>
<td>negq</td>
<td>dst = -dst</td>
<td>negate</td>
</tr>
<tr>
<td>notq</td>
<td>dst = ~dst</td>
<td>bitwise complement</td>
</tr>
</tbody>
</table>

- See CSPP Section 3.5.5 for more instructions: mulq, cqto, idivq, divq
### Arithmetic Example

```c
long simple_arith(long x, long y) {
    long t1 = x + y;
    long t2 = t1 * 3;
    return t2;
}
```

- **Register Use(s)**
  - `%rdi` 1st argument (x)
  - `%rsi` 2nd argument (y)
  - `%rax` return value

#### Simple Arithmetic

- `y += x;`
- `y *= 3;`
- `long r = y;`
- `return r;`

#### Assembly Code

```assembly
simple_arith:
    addq %rdi, %rsi
    imulq $3, %rsi
    movq %rsi, %rax
    ret
```

### Calling Convention

- **%rdi** 1st argument (x)
- **%rsi** 2nd argument (y)
- **%rax** return value
Example of Basic Addressing Modes

```c
void swap(long *xp, long *yp)
{
    long t0 = *xp;
    long t1 = *yp;
    *xp = t1;
    *yp = t0;
}
```

**swap**: $\text{src}, \text{dst}$ (AT&T syntax)
- `movq (%rdi), %rax`
- `movq (%rsi), %rdx`
- `movq %rdx, (%rdi)`
- `movq %rax, (%rsi)`
- `ret`

Mem operands
Understanding swap()

```c
void swap(long *xp, long *yp)
{
    long t0 = *xp;
    long t1 = *yp;
    *xp = t1;
    *yp = t0;
}
```

**Registers**

- %rdi
- %rsi
- %rax
- %rdx

**Memory**

**Register**  **Variable**

- %rdi ↔ xp
- %rsi ↔ yp
- %rax ↔ t0
- %rdx ↔ t1
Understanding swap()

Registers

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>%rdi</td>
<td>0x120</td>
</tr>
<tr>
<td>%rsi</td>
<td>0x100</td>
</tr>
<tr>
<td>%rax</td>
<td></td>
</tr>
<tr>
<td>%rdx</td>
<td></td>
</tr>
</tbody>
</table>

Memory

<table>
<thead>
<tr>
<th>Word Address</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x120</td>
<td>123</td>
</tr>
<tr>
<td>0x118</td>
<td></td>
</tr>
<tr>
<td>0x110</td>
<td></td>
</tr>
<tr>
<td>0x108</td>
<td></td>
</tr>
<tr>
<td>0x100</td>
<td>456</td>
</tr>
</tbody>
</table>

swap:

```
    movq (%rdi), %rax # t0 = *xp
    movq (%rsi), %rdx # t1 = *yp
    movq %rdx, (%rdi) # *xp = t1
    movq %rax, (%rsi) # *yp = t0
    ret
```
Understanding `swap()`

### Registers

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### Memory

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### swap:

```
movq (%rdi), %rax  # t0 = *xp
movq (%rsi), %rdx  # t1 = *yp
movq %rdx, (%rdi)  # *xp = t1
movq %rax, (%rsi)  # *yp = t0
ret
```
Understanding `swap()`

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### Memory

<table>
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</table>

### Word Address

- 0x120
- 0x118
- 0x110
- 0x108
- 0x100

### Assembly Code

```
swap:
  movq (%rdi), %rax  # t0 = *xp
  movq (%rsi), %rdx  # t1 = *yp
  movq %rdx, (%rdi)  # *xp = t1
  movq %rax, (%rsi)  # *yp = t0
  ret
```
Understanding `swap()`

**Registers**

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</table>

**Swap**

```
swap:
    movq (%rdi), %rax  # t0 = *xp
    movq (%rsi), %rdx  # t1 = *yp
    movq %rdx, (%rdi)  # *xp = t1
    movq %rax, (%rsi)  # *yp = t0
    ret
```
Understanding `swap()`

**Registers**

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<tr>
<td><code>%rdi</code></td>
<td>0x120</td>
</tr>
<tr>
<td><code>%rsi</code></td>
<td>0x100</td>
</tr>
<tr>
<td><code>%rax</code></td>
<td>123</td>
</tr>
<tr>
<td><code>%rdx</code></td>
<td>456</td>
</tr>
</tbody>
</table>

**Memory**

<table>
<thead>
<tr>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x120</td>
</tr>
<tr>
<td>0x118</td>
</tr>
<tr>
<td>0x110</td>
</tr>
<tr>
<td>0x108</td>
</tr>
<tr>
<td>0x100</td>
</tr>
</tbody>
</table>

These didn't change!

```plaintext
swap:
    movq (%rdi), %rax  # t0 = *xp
    movq (%rsi), %rdx  # t1 = *yp
    movq %rdx, (%rdi)  # *xp = t1
    movq %rax, (%rsi)  # *yp = t0
    ret
```
Memory Addressing Modes: Basic

- **Indirect:** \((R)\) \(\text{Mem}[\text{Reg}[R]]\)
  - Data in register \(R\) specifies the memory address
  - Like pointer dereference in C
  - **Example:** \(\text{movq } (\%rcx), \%rax\)

- **Displacement:** \(D(R)\) \(\text{Mem}[\text{Reg}[R]+D]\)
  - Data in register \(R\) specifies the *start* of some memory region
  - Constant displacement \(D\) specifies the offset from that address
  - **Example:** \(\text{movq } 8(\%rbp), \%rdx\)
Complete Memory Addressing Modes

**General:**

- **D(Rb, Ri, S)** $\text{Mem}[\text{Reg}[Rb] + \text{Reg}[Ri] \times S + D]$
  - Rb: Base register (any register)
  - Ri: Index register (any register except %rsp)
  - S: Scale factor (1, 2, 4, 8) – *why these numbers?*
  - D: Constant displacement value (a.k.a. immediate)

**Special cases** (see CSPP Figure 3.3 on p.181)

- **D(Rb, Ri)** $\text{Mem}[\text{Reg}[Rb] + \text{Reg}[Ri] + D]$ (S=1)
- **(Rb, Ri, S)** $\text{Mem}[\text{Reg}[Rb] + \text{Reg}[Ri] \times S]$ (D=0)
- **(Rb, Ri)** $\text{Mem}[\text{Reg}[Rb] + \text{Reg}[Ri]]$ (S=1, D=0)
- **(, Ri, S)** $\text{Mem}[\text{Reg}[Ri] \times S]$ (Rb=0, D=0)
Address Computation Examples

<table>
<thead>
<tr>
<th>Expression</th>
<th>Address Computation</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>$0x8(%rdx)$</td>
<td>$0xf008 + 0x8$</td>
<td>$0xf008$</td>
</tr>
<tr>
<td>$(%rdx, %rcx)$</td>
<td>$0xf000 + 0x0100$</td>
<td>$0xf100$</td>
</tr>
<tr>
<td>$(%rdx, %rcx, 4)$</td>
<td>$0xf000 + 0x0400$</td>
<td>$0xf400$</td>
</tr>
<tr>
<td>$0x80(+, %rdx, 2)$</td>
<td></td>
<td>$0x1e080$</td>
</tr>
</tbody>
</table>
Summary

- x86-64 is a complex instruction set computing (CISC) architecture
  - There are 3 types of operands in x86-64
    - Immediate, Register, Memory
  - There are 3 types of instructions in x86-64
    - Data transfer, Arithmetic, Control Flow

- **Memory Addressing Modes**: The addresses used for accessing memory in `mov` (and other) instructions can be computed in several different ways
  - *Base register, index register, scale factor, and displacement* map well to pointer arithmetic operations