1 Hit or Miss

Given these caches, do we hit or miss on the following accesses? If it's a hit, what value do we read?

Direct Mapped:

Set	Valid	Tag	B0	B1	B2	B3	Set	Valid	Tag	B0	B1	B2	B3
0	1	15	63	B4	C1	A4	8	0	-	-	-	-	-
1	0	-	-	-	-	-	9	1	0	1	12	23	34
2	0	-	-	-	-	-	10	1	1	98	89	CB	BC
3	1	0D	DE	AF	BA	DE	11	0	1E	4B	33	10	54
4	0	-	-	-	-	-	12	0	-	-	-	-	-
5	0	-	-	-	-	-	13	1	11	C0	4	39	AA
6	1	13	31	14	15	93	14	0	-	-	-	-	-
7	0	-	-	-	-	-	15	1	0F	FF	6F	30	0

2-Way Set Associative:

Set	Valid	Tag	B0	B1	B2	B3	Set	Valid	Tag	B0	B1	B2	B3
0	0	-	-	-	-	-	0	0	-	-	-	-	-
1	0	-	-	-	-	-	1	1	2F	1	20	40	3
2	1	3	4F	D4	A1	3B	2	1	0E	99	9	87	56
3	0	-	-	-	-	-	3	0	-	-	-	-	-
4	0	6	11	23	6A	42	4	0	-	-	-	-	-
5	1	21	DE	AD	BE	EF	5	0	-	-	-	-	-
6	0	-	-	-	-	-	6	1	37	22	B6	DB	AA
7	1	11	0	12	51	55	7	0	-	-	-	-	-

Fully Associative:

Set	Valid	Tag	B0	B1	B2	B3	Set	Valid	Tag	B0	B1	B2	B3
0	1	1F4	0	1	2	3	0	0	-	-	-	-	-
0	0	-	-	-	-	-	0	1	AB	2	30	44	67
0	1	100	F4	4D	EE	11	0	1	34	FD	EC	BA	23
0	0	77	12	23	34	45	0	0	-	-	-	-	-
0	0	-	-	-	-	-	0	1	1C6	0	11	22	33
0	1	101	DA	14	EE	22	0	1	45	67	78	89	9A
0	0	-	-	-	-	-	0	1	1	70	0	44	A6
0	1	16	90	32	AC	24	0	0	-	-	-	-	-

1.1 direct mapped:

- read `0x7AC`
- read `0x24`
- read `0x99F`

1.2 2-way set associative:

- read `0x435`
- read `0x388`
- read `0xOD3`

1.3 fully associative:

- read `0x1DD`
- read `0x719`
- read `0x2AA`

2 Benedict Cumbercache

Given the following sequence of access results (addresses are given in decimal) on an empty cache of size 16 bytes, what can we *deduce* about its properties? Assume an LRU replacement policy.

`(0, Miss), (8, Miss), (0, Hit), (16, Miss), (8, Miss)`

2.1 What can we say about the block size?

2.2 What is this cache's associativity?

2.3 How many sets could this cache have?

2.4 How many bits will the tag use given an n-bit address?

3 Miss Rates

Consider the following code. Assuming cache size 1 KB, direct-mapped, 16B block size, what is the miss rate?

```
for (int i = 0; i < 64; i++) {
    for (int j = 0; j < 64; j++) {
        array[i][j] = 0;
    }
}
```

3.1 In the previous example, what code modifications can change the miss rate?

3.2 What cache changes can changes the miss rate?

- Changing the cache size?
- Changing the associativity?
- Changing the block size?