Roadmap

C:
car *c = malloc(sizeof(car));
c->miles = 100;
c->gals = 17;
float mpg = get_mpg(c);
free(c);

Java:
Car c = new Car();
c.setMiles(100);
c.setGals(17);
float mpg =
c.getMPG();

Assembly language:
get_mpg:
pushq %rbp
movq %rsp, %rbp
...
popq %rbp
ret

Machine code:
0111010000011000
100011010000010000000010
1000100111000010
110000011111110100001111

Computer system:
OS:
Windows 8
Mac

Memory & data
Integers & floats
Machine code & C
x86 assembly
Procedures & stacks
Arrays & structs
Memory & caches
Processes
Virtual memory
Memory allocation
Java vs. C

Spring 2014
Again: Processes

- Definition: A *process* is an instance of a running program
  - One of the most important ideas in computer science
  - Not the same as “program” or “processor”

- Process provides each program with **two key abstractions**:
  - Logical control flow
    - Each process seems to have exclusive use of the CPU
  - Private virtual address space
    - Each process seems to have exclusive use of main memory

- How are these illusions maintained?
  - Process executions interleaved (multi-tasking) – done...
  - Address spaces managed by virtual memory system – now!
Virtual Memory (VM)

- Overview and motivation
- VM as tool for caching
- Address translation
- VM as tool for memory management
- VM as tool for memory protection
Memory as we know it so far... is virtual!

- Programs refer to *virtual* memory addresses
  - `movl (%ecx),%eax`
  - Conceptually memory is just a very large array of bytes
  - Each byte has its own address
  - System provides address space private to particular “process”

- Allocation: Compiler and run-time system
  - Where different program objects should be stored
  - All allocation within single virtual address space

- But...
  - We probably don’t have exactly $2^w$ bytes of physical memory.
  - *We certainly* don’t have $2^w$ bytes of physical memory for every process.
  - We have multiple processes that usually should not interfere with each other, but sometimes should share code or data.
Problem 1: How Does Everything Fit?

64-bit addresses can address several exabytes
(18,446,744,073,709,551,616 bytes)

Physical main memory offers a few gigabytes
(e.g. 8,589,934,592 bytes)

1 virtual address space per process, with many processes...

(Actually, it’s smaller than that dot compared to virtual memory.)
Problem 2: Memory Management

Process 1
Process 2
Process 3
...
Process n

stack
heap
.text
.data
...

Physical main memory

What goes where?
Problem 3: How To Protect

Physical main memory

Process i

Process j

Problem 4: How To Share?

Physical main memory

Process i

Process j
How can we solve these problems?
Indirection

- “Any problem in computer science can be solved by adding another level of indirection.” –David Wheeler, inventor of the subroutine (a.k.a. procedure)

- **Without Indirection**

- **With Indirection**

  What if I want to move Thing?
Indirection

- **Indirection**: the ability to reference something using a name, reference, or container instead the value itself. A flexible mapping between a name and a thing allows changing the thing without notifying holders of the name.

- **Without Indirection**

- **With Indirection**

- **Examples of indirection**:
  - Domain Name Service (DNS): translation from name to IP address
  - phone system: cell phone number portability
  - snail mail: mail forwarding
  - 911: routed to local office
  - Dynamic Host Configuration Protocol (DHCP): local network address assignment
  - call centers: route calls to available operators, etc.
Indirection in Virtual Memory

- Each process gets its own private virtual address space
- Solves the previous problems
Address Spaces

- **Virtual address space:** Set of $N = 2^n$ virtual addresses
  \{0, 1, 2, 3, ..., N-1\}

- **Physical address space:** Set of $M = 2^m$ physical addresses ($n \geq m$)
  \{0, 1, 2, 3, ..., M-1\}

- Every byte in main memory has:
  - one physical address
  - zero, one, *or more* virtual addresses
A virtual address can be mapped to either physical memory or disk.
A System Using Physical Addressing

- Used in “simple” systems with (usually) just one process:
  - embedded microcontrollers in devices like cars, elevators, and digital picture frames
A System Using Virtual Addressing

- Physical addresses are *completely invisible to programs*.
- Used in all modern desktops, laptops, servers, smartphones...
- One of the great ideas in computer science
Why Virtual Memory (VM)?

- **Efficient use of limited main memory (RAM)**
  - Use RAM as a cache for the parts of a virtual address space
    - some non-cached parts stored on disk
    - some (unallocated) non-cached parts stored nowhere
  - Keep only active areas of virtual address space in memory
    - transfer data back and forth as needed

- **Simplifies memory management for programmers**
  - Each process gets the same full, private linear address space

- **Isolates address spaces**
  - One process can’t interfere with another’s memory
    - because they operate in different address spaces
  - User process cannot access privileged information
    - different sections of address spaces have different permissions
VM and the Memory Hierarchy

- Think of virtual memory as array of \( N = 2^n \) contiguous bytes.
- Pages of virtual memory are usually stored in physical memory, but sometimes spill to disk.
  - Pages are another unit of aligned memory (size is \( P = 2^p \) bytes)
  - Each virtual page can be stored in any physical page.
or: Virtual Memory as DRAM Cache for Disk

- Think of virtual memory as an array of \( N = 2^n \) contiguous bytes stored on a disk.
- Then physical main memory is used as a cache for the virtual memory array
  - The cache blocks are called pages (size is \( P = 2^p \) bytes)
Memory Hierarchy: Core 2 Duo

**Not drawn to scale**

- **SRAM**
  - L1 I-cache
  - L1 D-cache
  - 32 KB

- **DRAM**
  - L2 unified cache
  - ~4 MB

- **Main Memory**
  - ~4 GB

- **Disk**
  - ~500 GB

**Throughput:**
- CPU Reg
- SRAM: 16 B/cycle
- L1 I-cache: 8 B/cycle
- L1 D-cache: 2 B/cycle
- L2 unified cache: 1 B/30 cycles

**Latency:**
- CPU Reg
- SRAM: 3 cycles
- L1 I-cache: 14 cycles
- L1 D-cache: 100 cycles
- L2 unified cache: millions of cycles

**Miss penalty (latency):**
- SRAM: 33x
- DRAM: 10,000x
Virtual Memory Design Consequences

- Large page size: typically 4-8 KB, sometimes up to 4 MB
- Fully associative
  - Any virtual page can be placed in any physical page
  - Requires a “large” mapping function – different from CPU caches
- Highly sophisticated, expensive replacement algorithms in OS
  - Too complicated and open-ended to be implemented in hardware
- Write-back rather than write-through
Address Translation

How do we perform the virtual -> physical address translation?
Address Translation: Page Tables

- A page table is an array of page table entries (PTEs) that maps virtual pages to physical pages.

How many page tables are in the system? One per process
Address Translation With a Page Table

In most cases, the hardware (the MMU) can perform this translation on its own, without software assistance.

This feels familiar…
Page Hit

- **Page hit**: reference to VM byte that is in physical memory
Page Fault

- **Page fault**: reference to VM byte that is **NOT** in physical memory

What happens when a page fault occurs?
Fault Example: Page Fault

- User writes to memory location
- That portion (page) of user’s memory is currently on disk

User Process

\[
\text{movl} \quad \text{exception: page fault}
\]

OS

\[
\text{Create page and load into memory}
\]

- Page handler must load page into physical memory
- Returns to faulting instruction: \textbf{mov} is executed \textit{again}!
- Successful on second try

```c
int a[1000];
main ()
{
    a[500] = 13;
}
```

Virtual Memory
Handling Page Fault

- Page miss causes page fault (an exception)
Handling Page Fault

- Page miss causes page fault (an exception)
- Page fault handler selects a *victim* to be evicted (here VP 4)
Handling Page Fault

- Page miss causes page fault (an exception)
- Page fault handler selects a *victim* to be evicted (here VP 4)

![Diagram of page fault handling]

- Memory resident page table (DRAM)
- Physical page number or disk address
- Physical memory (DRAM)
- Virtual memory (disk)
Handling Page Fault

- Page miss causes page fault (an exception)
- Page fault handler selects a *victim* to be evicted (here VP 4)
- Offending instruction is restarted: page hit!
Why does it work?
Why does VM work on RAM/disk? Locality.

- Virtual memory works well for avoiding disk accesses because of locality
  - Same reason that L1 / L2 / L3 caches work

- The set of virtual pages that a program is “actively” accessing at any point in time is called its **working set**
  - Programs with better temporal locality will have smaller working sets

- If (working set size of one process < main memory size):
  - Good performance for one process after compulsory misses

- But if
  - **Thrashing**: Performance meltdown where pages are swapped (copied) between memory and disk continuously. CPU always waiting or paging.
  - Full quote: “Every problem in computer science can be solved by adding another level of indirection, but that usually will create another problem.”
Simplifying Linking and Loading

**Linking**
- Each program has similar virtual address space
- Code, stack, and shared libraries start at the same address

**Loading**
- `execve()` allocates virtual pages for `.text` and `.data` sections
  - Creates PTEs marked as invalid
- The `.text` and `.data` sections are copied, page by page, on demand by the virtual memory system
VM for Managing Multiple Processes

- Key abstraction: each process has its own virtual address space
  - It can view memory as a simple linear array
- With virtual memory, this simple linear virtual address space need not be contiguous in physical memory
  - Process needs to store data in another VP? Just map it to any PP!

![Diagram of virtual memory addressing]

Virtual Address Space for Process 1:
- Virtual Address Space: VP 1, VP 2, ..., VP N-1
- Address translation
- Physical Address Space (DRAM): PP 2, PP 6, PP 8, ..., PP M-1

Virtual Address Space for Process 2:
- Virtual Address Space: VP 1, VP 2, ..., VP N-1
- Address translation
- Physical Address Space (DRAM): PP 2, PP 6, PP 8, ..., PP M-1
VM for Protection and Sharing

- The mapping of VPs to PPs provides a simple mechanism to protect memory and to share memory between processes.
  - **Sharing**: just map virtual pages in separate address spaces to the same physical page (here: PP 6)
  - **Protection**: process simply can’t access physical pages to which none of its virtual pages are mapped (here: Process 2 can’t access PP 2).
Memory Protection Within a Single Process

- Can we use virtual memory to control read/write/execute permissions? How?
Memory Protection Within a Single Process

- Extend page table entries with permission bits
- MMU checks these permission bits on every memory access
  - If violated, raises exception and OS sends SIGSEGV signal to process (segmentation fault)

**Process i:**

<table>
<thead>
<tr>
<th>VP 0:</th>
<th>Valid</th>
<th>READ</th>
<th>WRITE</th>
<th>EXEC</th>
<th>Physical Page Num</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>PP 6</td>
</tr>
<tr>
<td>VP 1:</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>PP 4</td>
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<tr>
<td>VP 2:</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>PP 2</td>
</tr>
</tbody>
</table>

**Process j:**

<table>
<thead>
<tr>
<th>VP 0:</th>
<th>Valid</th>
<th>READ</th>
<th>WRITE</th>
<th>EXEC</th>
<th>Physical Page Num</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>PP 9</td>
</tr>
<tr>
<td>VP 1:</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>PP 6</td>
</tr>
<tr>
<td>VP 2:</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>PP 11</td>
</tr>
</tbody>
</table>

Spring 2014 Virtual Memory
Terminology

- **context switch**
  - Switch between processes on the same CPU

- **page in**
  - Move pages of virtual memory from disk to physical memory

- **page out**
  - Move pages of virtual memory from physical memory to disk

- **thrash**
  - Total working set size of processes is larger than physical memory
  - Most time is spent paging in and out instead of doing useful computation
Address Translation: Page Hit

1) Processor sends virtual address to MMU (*memory management unit*)
2-3) MMU fetches PTE from page table in cache/memory
4) MMU sends physical address to cache/memory
5) Cache/memory sends data word to processor
1) Processor sends virtual address to MMU
2-3) MMU fetches PTE from page table in cache/memory
4) Valid bit is zero, so MMU triggers page fault exception
5) Handler identifies victim (and, if dirty, pages it out to disk)
6) Handler pages in new page and updates PTE in memory
7) Handler returns to original process, restarting faulting instruction
Hmm... Translation Sounds Slow!

- The MMU accesses memory *twice*: once to first get the PTE for translation, and then again for the actual memory request from the CPU
  - The PTEs *may* be cached in L1 like any other memory word
    - But they may be evicted by other data references
    - And a hit in the L1 cache still requires 1-3 cycles

- *What can we do to make this faster?*
Speeding up Translation with a TLB

- **Solution:** add another cache!

- **Translation Lookaside Buffer (TLB):**
  - Small hardware cache in MMU
  - Maps virtual page numbers to physical page numbers
  - Contains complete *page table entries* for small number of pages
    - Modern Intel processors: 128 or 256 entries in TLB
  - Much faster than a page table lookup in cache/memory
TLB Hit

A TLB hit eliminates a memory access
A TLB miss incurs an additional memory access (the PTE)
Fortunately, TLB misses are rare. **Does a TLB miss require disk access?**
Simple Memory System Example (small)

Addressing
- 14-bit virtual addresses
- 12-bit physical address
- Page size = 64 bytes

Virtual Page Number (VPN) -> Virtual Page Offset (VPO)

Physical Page Number (PPN) -> Physical Page Offset (PPO)
Simple Memory System Page Table

- Only showing first 16 entries (out of $256 = 2^8$)

<table>
<thead>
<tr>
<th>VPN</th>
<th>PPN</th>
<th>Valid</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>28</td>
<td>1</td>
</tr>
<tr>
<td>01</td>
<td>–</td>
<td>0</td>
</tr>
<tr>
<td>02</td>
<td>33</td>
<td>1</td>
</tr>
<tr>
<td>03</td>
<td>02</td>
<td>1</td>
</tr>
<tr>
<td>04</td>
<td>–</td>
<td>0</td>
</tr>
<tr>
<td>05</td>
<td>16</td>
<td>1</td>
</tr>
<tr>
<td>06</td>
<td>–</td>
<td>0</td>
</tr>
<tr>
<td>07</td>
<td>–</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VPN</th>
<th>PPN</th>
<th>Valid</th>
</tr>
</thead>
<tbody>
<tr>
<td>08</td>
<td>13</td>
<td>1</td>
</tr>
<tr>
<td>09</td>
<td>17</td>
<td>1</td>
</tr>
<tr>
<td>0A</td>
<td>09</td>
<td>1</td>
</tr>
<tr>
<td>0B</td>
<td>–</td>
<td>0</td>
</tr>
<tr>
<td>0C</td>
<td>–</td>
<td>0</td>
</tr>
<tr>
<td>0D</td>
<td>2D</td>
<td>1</td>
</tr>
<tr>
<td>0E</td>
<td>11</td>
<td>1</td>
</tr>
<tr>
<td>0F</td>
<td>0D</td>
<td>1</td>
</tr>
</tbody>
</table>

- What about a real address space? Read more in the book...
Simple Memory System TLB

- **16 entries**
- **4-way associative**

---

**TLB ignores page offset. Why?**

---

<table>
<thead>
<tr>
<th>Set</th>
<th>Tag</th>
<th>PPN</th>
<th>Valid</th>
<th>Tag</th>
<th>PPN</th>
<th>Valid</th>
<th>Tag</th>
<th>PPN</th>
<th>Valid</th>
<th>Tag</th>
<th>PPN</th>
<th>Valid</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>03</td>
<td>–</td>
<td>0</td>
<td>09</td>
<td>0D</td>
<td>1</td>
<td>00</td>
<td>–</td>
<td>0</td>
<td>07</td>
<td>02</td>
<td>1</td>
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<td>1</td>
<td>03</td>
<td>2D</td>
<td>1</td>
<td>02</td>
<td>–</td>
<td>0</td>
<td>04</td>
<td>–</td>
<td>0</td>
<td>0A</td>
<td>–</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>02</td>
<td>–</td>
<td>0</td>
<td>08</td>
<td>–</td>
<td>0</td>
<td>06</td>
<td>–</td>
<td>0</td>
<td>03</td>
<td>–</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>07</td>
<td>–</td>
<td>0</td>
<td>03</td>
<td>0D</td>
<td>1</td>
<td>0A</td>
<td>34</td>
<td>1</td>
<td>02</td>
<td>–</td>
<td>0</td>
</tr>
</tbody>
</table>
## Simple Memory System Cache

- 16 lines, 4-byte block size
- Physically addressed
- Direct mapped

### Cache Addressing

<table>
<thead>
<tr>
<th>Physical Page Number</th>
<th>Physical Page Offset</th>
<th>Cache Index</th>
<th>Cache Offset</th>
<th>Cache Tag</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>00</td>
<td>0</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>1</td>
<td>01</td>
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<tr>
<td>2</td>
<td>02</td>
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<td>02</td>
<td>02</td>
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<tr>
<td>3</td>
<td>03</td>
<td>3</td>
<td>03</td>
<td>03</td>
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<tr>
<td>4</td>
<td>04</td>
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</tr>
<tr>
<td>7</td>
<td>07</td>
<td>7</td>
<td>07</td>
<td>07</td>
</tr>
</tbody>
</table>

### Example Table

<table>
<thead>
<tr>
<th>Idx</th>
<th>Tag</th>
<th>Valid</th>
<th>B0</th>
<th>B1</th>
<th>B2</th>
<th>B3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>19</td>
<td>1</td>
<td>99</td>
<td>11</td>
<td>23</td>
<td>11</td>
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<td>1</td>
<td>15</td>
<td>0</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>2</td>
<td>1B</td>
<td>1</td>
<td>00</td>
<td>02</td>
<td>04</td>
<td>08</td>
</tr>
<tr>
<td>3</td>
<td>36</td>
<td>0</td>
<td>–</td>
<td>–</td>
<td>–</td>
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<tr>
<td>4</td>
<td>32</td>
<td>1</td>
<td>43</td>
<td>6D</td>
<td>8F</td>
<td>09</td>
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<td>1</td>
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<td>F0</td>
<td>1D</td>
</tr>
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<td>6</td>
<td>31</td>
<td>0</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
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<td>7</td>
<td>16</td>
<td>1</td>
<td>11</td>
<td>C2</td>
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</tr>
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</table>

### Example Table (Second Half)

<table>
<thead>
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<th>B0</th>
<th>B1</th>
<th>B2</th>
<th>B3</th>
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<tr>
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<td>–</td>
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<td>3B</td>
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<td>0</td>
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<td>–</td>
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<td>–</td>
</tr>
<tr>
<td>C</td>
<td>12</td>
<td>0</td>
<td>–</td>
<td>–</td>
<td>–</td>
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</tr>
<tr>
<td>D</td>
<td>16</td>
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</tr>
<tr>
<td>E</td>
<td>13</td>
<td>1</td>
<td>83</td>
<td>77</td>
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</tr>
</tbody>
</table>
### Current state of caches/tables

#### TLB

<table>
<thead>
<tr>
<th>Set</th>
<th>Tag</th>
<th>PPN</th>
<th>Valid</th>
<th>Tag</th>
<th>PPN</th>
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#### Cache

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<th>B2</th>
<th>B3</th>
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</tbody>
</table>
Address Translation Example #1

Virtual Address: 0x03D4

Virtual Address:

13 12 11 10 9 8 7 6 5 4 3 2 1 0

0 0 0 0 1 1 1 1 0 1 0 1 0 0

VPN 0x0F TLBI 3 TLBT 0x03 TLB Hit? Y Page Fault? N PPN: 0x0D

Physical Address:

11 10 9 8 7 6 5 4 3 2 1 0

0 0 1 1 0 1 0 1 0 1 0 0

CO 0 CI 0x5 CT 0x0D Hit? Y Byte: 0x36
Address Translation Example #2

Virtual Address: \(0x0B8F\)

```
  13 12 11 10  9  8  7  6  5  4  3  2  1 0
0 0 1 0 1 1 1 0 0 0 1 1 1 1
```

VPN: \(0x2E\)  TLBI: \(2\)  TLBT: \(0x0B\)  TLB Hit?: N  Page Fault?: Y  PPN: TBD

Physical Address

```
  11 10  9  8  7  6  5  4  3  2  1 0
```

CO: \_
Cl: 
CT: 
Hit?: 
Byte: 

PPN: 
PPO: 

Spring 2014  Virtual Memory
Address Translation Example #3

Virtual Address: 0x0020

<table>
<thead>
<tr>
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<th>12</th>
<th>11</th>
<th>10</th>
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<th>8</th>
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<td>1</td>
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</table>

VPN: 0x0000
TLBI: 0
TLBT: 0x00
TLB Hit?: N
Page Fault?: N
PPN: 0x28

Physical Address

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<tr>
<th>12</th>
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<th>8</th>
<th>7</th>
<th>6</th>
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PPN: 0
Cl: 0x8
CT: 0x28
Hit?: N
Byte: Mem
Servicing a Page Fault

- **(1) Processor signals disk controller**
  - Read block of length P starting at disk address X
  - Store starting at memory address Y

- **(2) Read occurs**
  - Direct Memory Access (DMA)
  - Under control of I/O controller

- **(3) Controller signals completion**
  - Interrupts processor
  - OS resumes suspended process
Summary

- **Programmer’s view of virtual memory**
  - Each process has its own private linear address space
  - Cannot be corrupted by other processes

- **System view of virtual memory**
  - Uses memory efficiently by caching virtual memory pages
    - Efficient only because of locality
  - Simplifies memory management and sharing
  - Simplifies protection by providing a convenient interpositioning point to check permissions
Memory System Summary

- **L1/L2 Memory Cache**
  - Purely a speed-up technique
  - Behavior invisible to application programmer and (mostly) OS
  - Implemented totally in hardware

- **Virtual Memory**
  - Supports many OS-related functions
    - Process creation, task switching, protection
  - Operating System (software)
    - Allocates/shares physical memory among processes
    - Maintains high-level tables tracking memory type, source, sharing
    - Handles exceptions, fills in hardware-defined mapping tables
  - Hardware
    - Translates virtual addresses via mapping tables, enforcing permissions
    - Accelerates mapping via translation cache (TLB)
Memory System Summary

- L1/L2 Memory Cache
  - Controlled by hardware
  - Programmer cannot control it
  - Programmer *can* write code in a way that takes advantage of it

- Virtual Memory
  - Controlled by OS and hardware
  - Programmer cannot control mapping to physical memory
  - Programmer can control sharing and some protection
    - via OS functions (not in 351)