Lecture Notes for Week 2

Thomas Issues

- Productivity Crisis
- Timing

→ Recommends Bottom-Up and "COT" Approach to Systems Houses

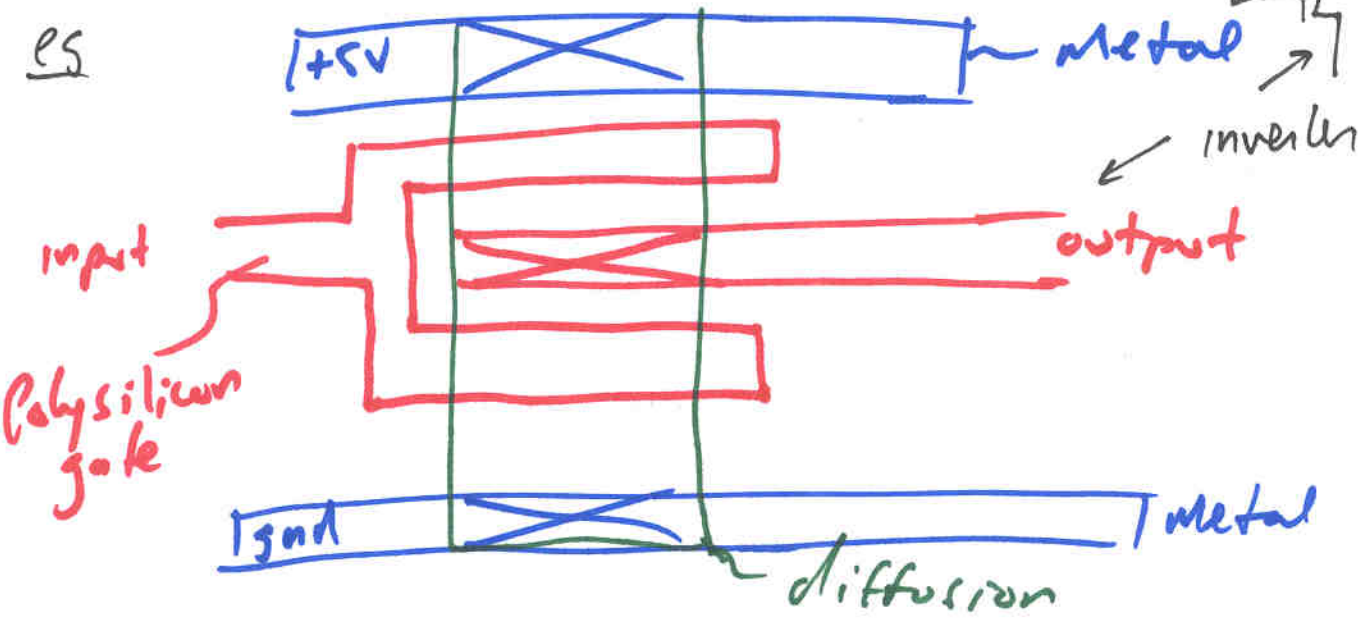
I say - Productivity Crisis
not new (Moore's Law)
but there is a <u>new</u> aspect to it:
VLSI is now an n-company problem

Timing presents new challenges in the handoff between Systems Houses and foundries (ASIC vendor)

Historical Perspective

(IC) VLSI is a lithographic process - need masks (optical) to make geometrical patterns on a silicon surface

ex: in → out



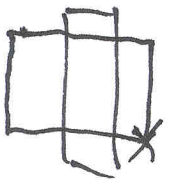
original Design methodology: exacto knife on Ruby Lith

let to productivity Crisis (P.C.)

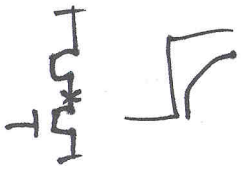
Solution: Add Computer Drawn Layout:

Designers could create more polygons than could be practically verified for physical design rules and adherence to the desired circuit schematic (light Table)

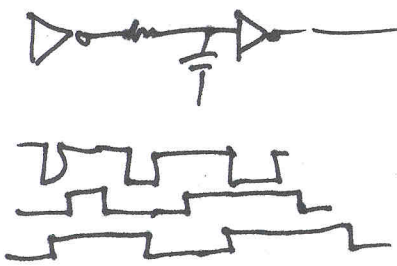
Solution: Add DRC (Design Rule checking) and LVS (Layout versus Schematic comparison)



Next bottleneck: Need to verify schematics through simulation at detailed level (spice w/ parasitics) and at abstract levels (logic, switch level)



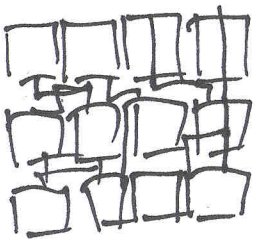
Solution: Add spice, parasitic (R,C) extraction from layout, logic and switch simulation.



up until this point, Ic design is mainly a 1-company problem: e.g. TI owns fab, Design SW, and performs all design tasks. Systems companies use standards parts such as memories, processors, small packages of gates, programmable logic devices, etc.

next bottle neck: too many individual transistors to design separately. And physical design too complex

Solution: Reuse — design blocks as cell libraries
design skill as place and route technologies

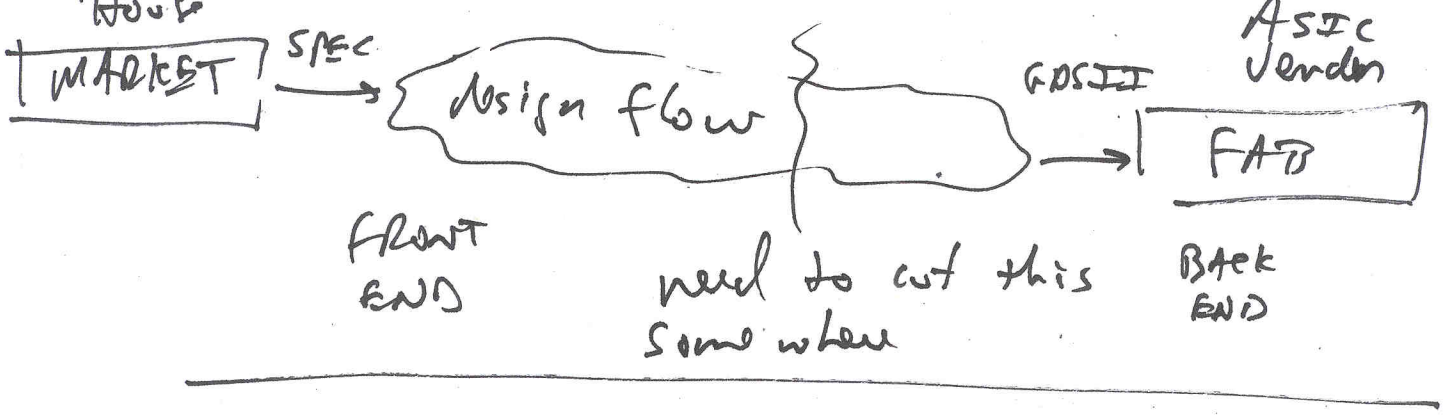


At this time, systems houses want "Application specific" IC's. Fabs too expensive to be "captive" need to market to many customers →

Solution: The ASIC Vendor Business Model

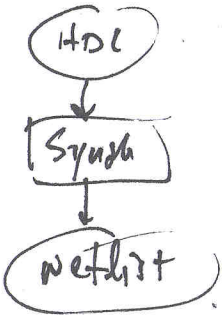
systems house: Perform logic design (front end)
ASIC Vendor: Provide cell library and Physical Design Services.

—— Now it becomes a 2 party problem ——

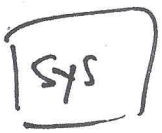


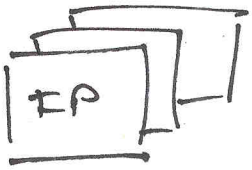
Next Productivity Bottleneck: too many gates need to specify function at a high level and synthesize at netlist:

Solution: Logic Synthesis Algorithms and Hardware Description Languages (HDL's)
Result is the mature ASIC Business model + Design Process.
(See attached Flow Diagram)

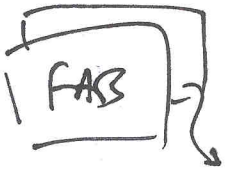


NEXT PROBLEM: NO systems company / or ASIC vendor has enough IP to fill existing die area: need to use outside IP.
becomes N-party problem





Sys must choose:
Do physical integration or leave it to FAB?



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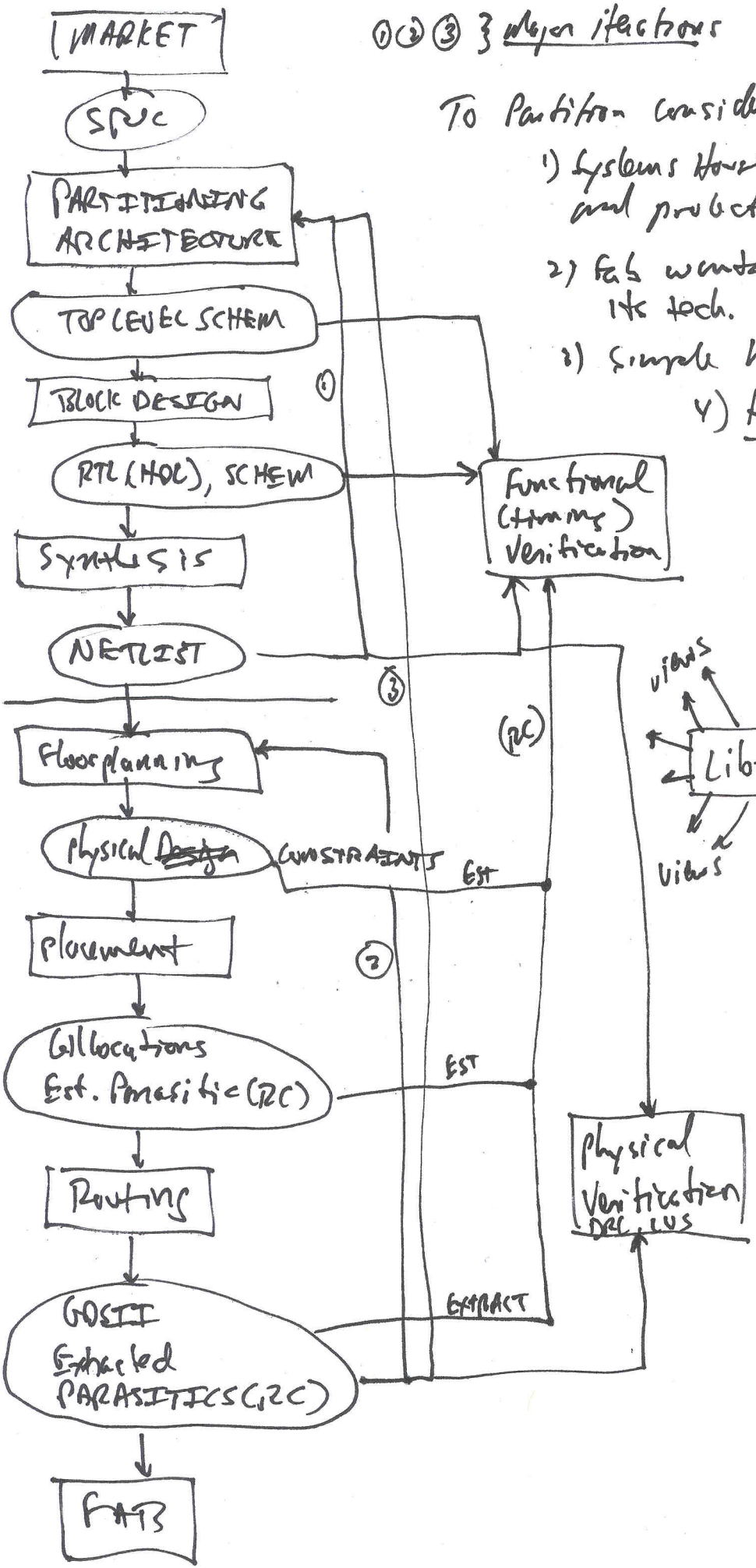


① ② ③ 3 major interfaces

To Partition consider:

1) Systems House wants to develop and protect IP
2) Fab wants to make access to its tech. easy
3) Simple handoff
4) Few iterations

so cut between netlist and floorplanning (logical/physical).

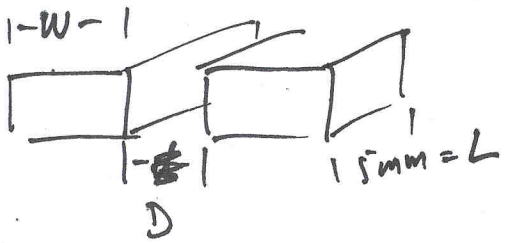
Standard ASIC MODEL

Problem 2 — Timing Problem: increase % path delay due to nets instead of gates

Exercise

	C_{area}	C_{fringe}	Ω/square	W	H	D
Tech 1	$19aF/mm^2$	$57aF/mm$	.06	2	.5	2
Tech 2	$17aF/mm^2$	$76aF/mm$	.07 Ω/square	1	1	1

given 5mm x w wires, with one minimum distance (D) neighbor determine



$\varepsilon_c = 3.45\ F/m$

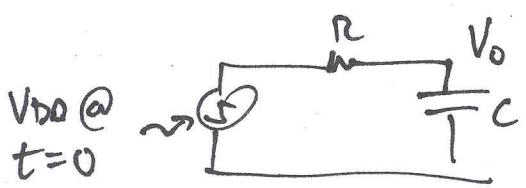
$\varepsilon_r = 3.9$

$$C_{TOT} = (W \times L) C_a + 2L C_f + \frac{A}{D} \varepsilon_0 \varepsilon_r$$

For Tech 1: $C_{TOT} = 92F \times 10^{-13} f$ $R = 150\Omega$ so $RC = 138ps$

For Tech 2: $C_{TOT} = 1.6 \times 10^{-12} F$ $R = 350\Omega$ so $RC = \underline{560ps}$

RC = time for



RC = time for V_0 to reach .63 V_{DD} after t=0, for step function input

Actual driver is not a step function

for Tech 1: Rise time = 650 ps

for Tech 2: Rise time = 150 ps

<u>Use spice simulations</u> attached to compare net delay to switching time (intrinsic or "gate" delay).

	gate	net	% net
Tech 1	650 ps	57 ps	
Tech 2	150 ps	316 ps	

Other observations from spice simulations

1. in Tech 1: distributed net model is about 9% - 10% faster than lumped net model. So use lumped and have a good margin!

but in Tech 2: distributed is about 50% faster than lumped: too much need detailed net model for accurate timing!

2. Coupling is significant in Tech 2 (~30%) but is negligible in Tech 1!

conclusion: no longer feasible to
divide between logical and
physical Design ("ASIC HANDOFF")

Sysco Houses must choose:
Do it all, or farm it out:
risk "Hollowing" out.

COT: Sysco House responsible for
library + Tools, fab only
contracts out raw foundry
access.