Introduction to CMOS VLSI Design

Layout, Fabrication, and Elementary Logic Design

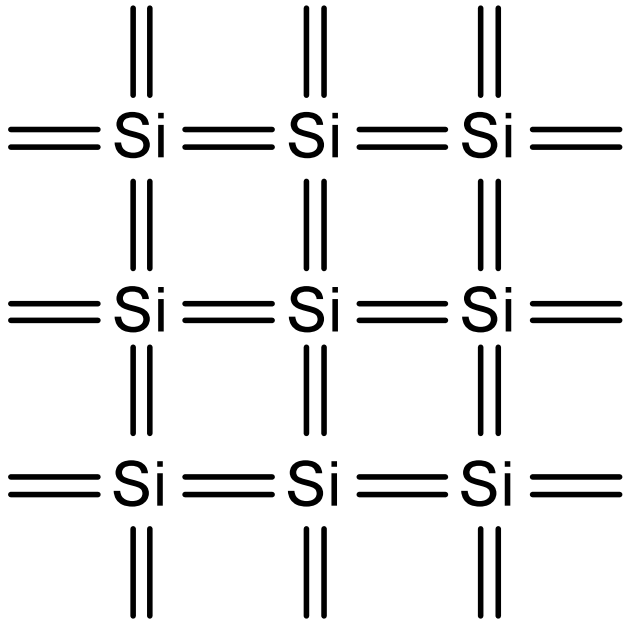
Adapted from Weste & Harris
CMOS VLSI Design

Overview

- Implementing switches with CMOS transistors
- How to compute logic functions with switches
- Fabricating transistors on a silicon wafer and connecting them together

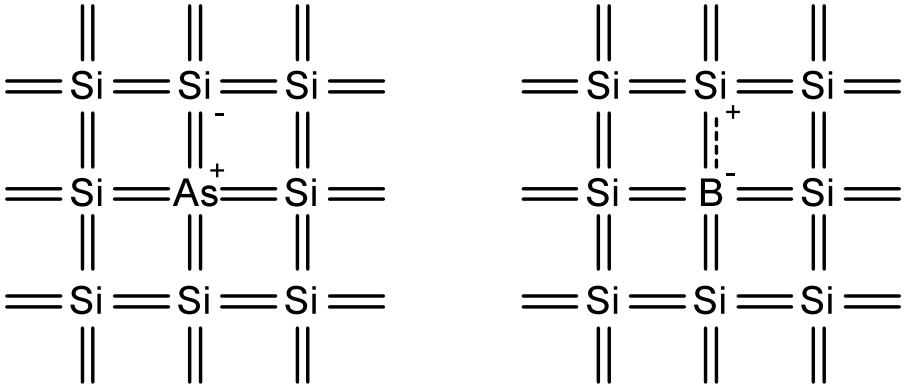
Silicon Lattice

- Transistors are built on a silicon substrate
- Silicon is a Group IV material
- Forms crystal lattice with bonds to four neighbors



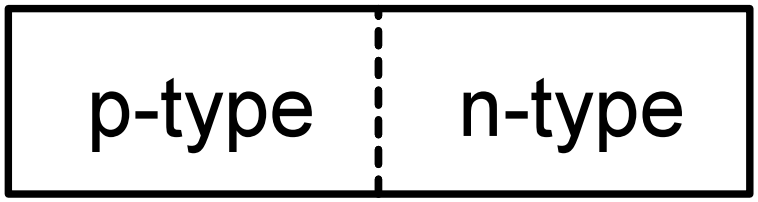
Dopants

- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants increases the conductivity
- Group V: extra electron (n-type)
- Group III: missing electron, called hole (p-type)

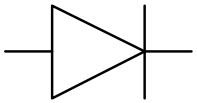


p-n Junctions

- A junction between p-type and n-type semiconductor forms a diode.
- Current flows only in one direction

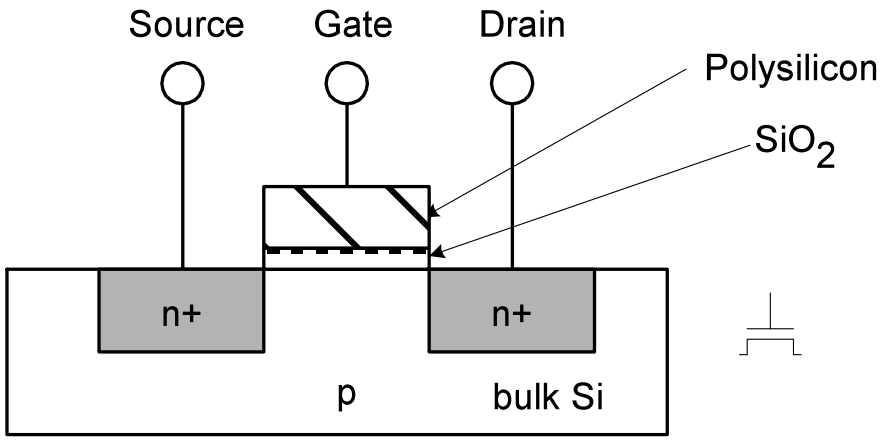


anode cathode



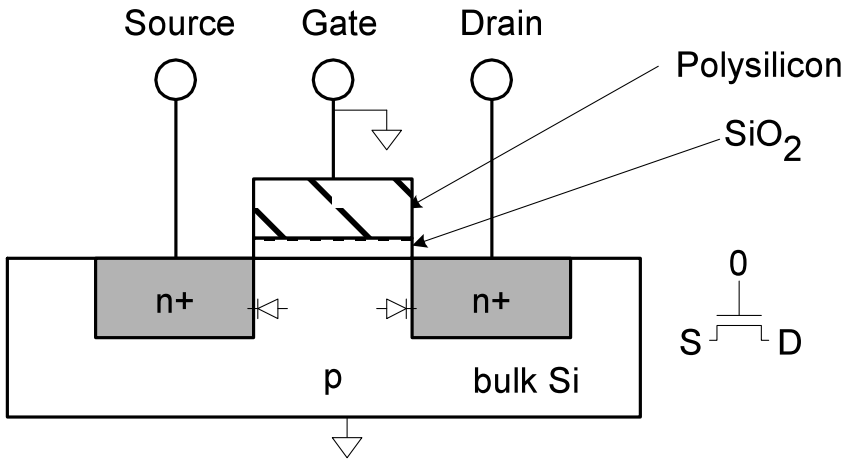
nMOS Transistor

- Four terminals: gate, source, drain, body
- Gate – oxide – body stack looks like a capacitor
  - Gate and body are conductors
  - SiO_2 (oxide) is a very good insulator



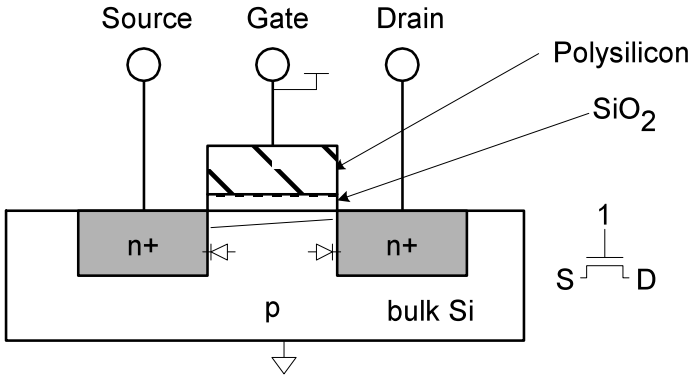
nMOS Operation

- Body is commonly tied to ground (0 V)
- When the gate is at a low voltage:
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF



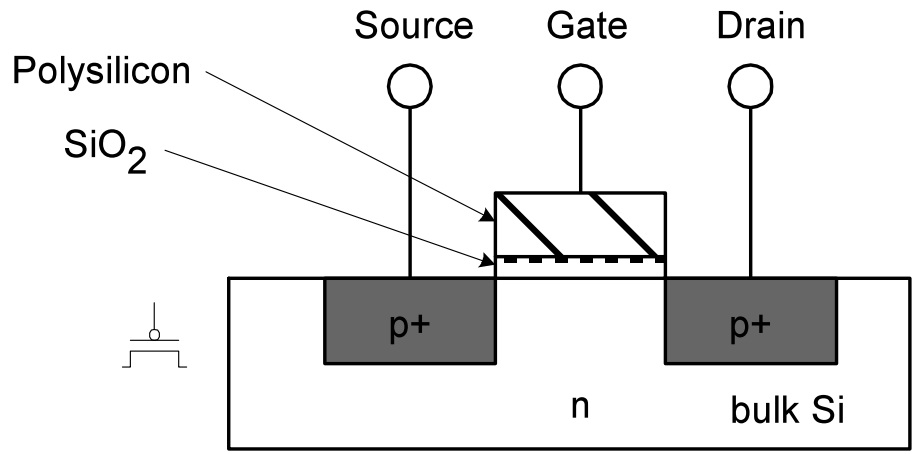
nMOS Operation

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON



pMOS Transistor

- Similar, but doping and voltages reversed
  - Body tied to high voltage (V_{DD})
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior

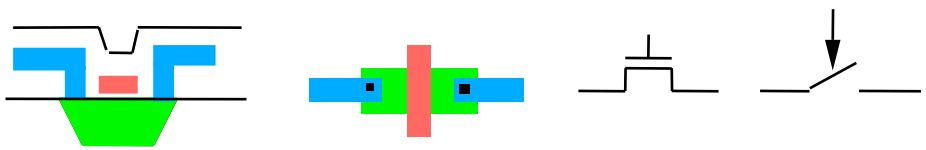


Power Supply Voltage

- GND = 0 V
- In 1980's, V_{DD} = 5V
- V_{DD} has decreased in modern processes
  - High V_{DD} would damage modern tiny transistors
  - Lower V_{DD} saves power
- V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, …

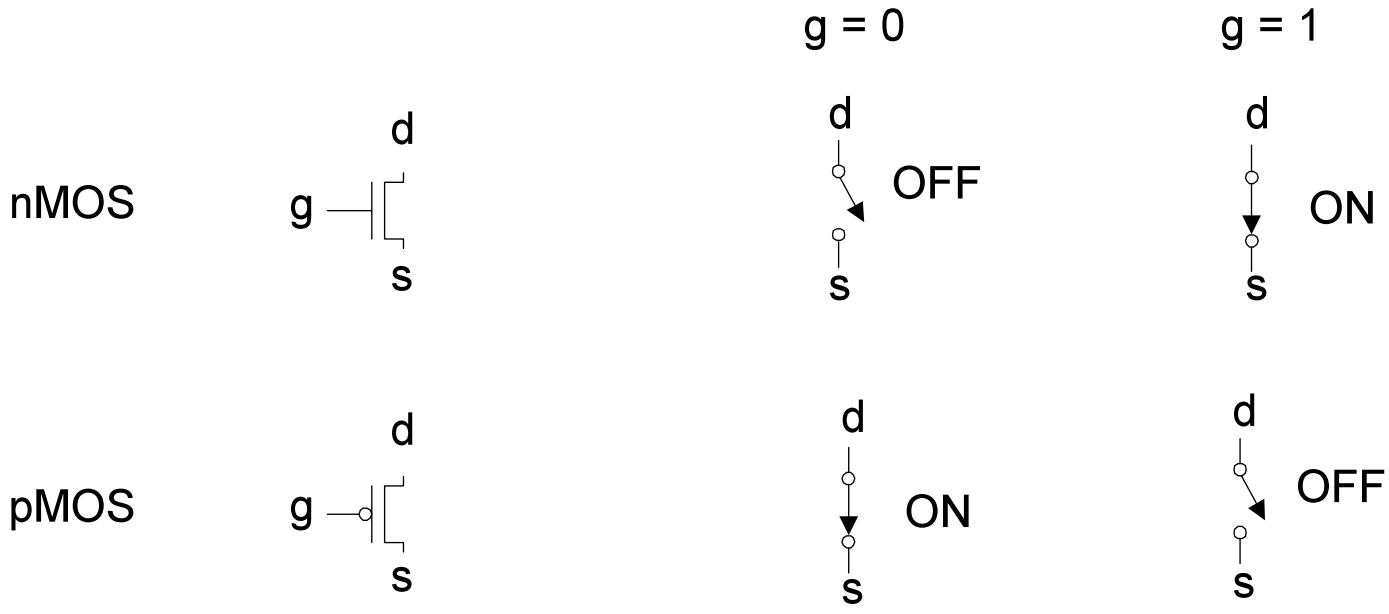
Transistor Abstraction

- 3D structure formed by fabrication
- 2D planar “layout” view
- Schematic symbol
- Switch

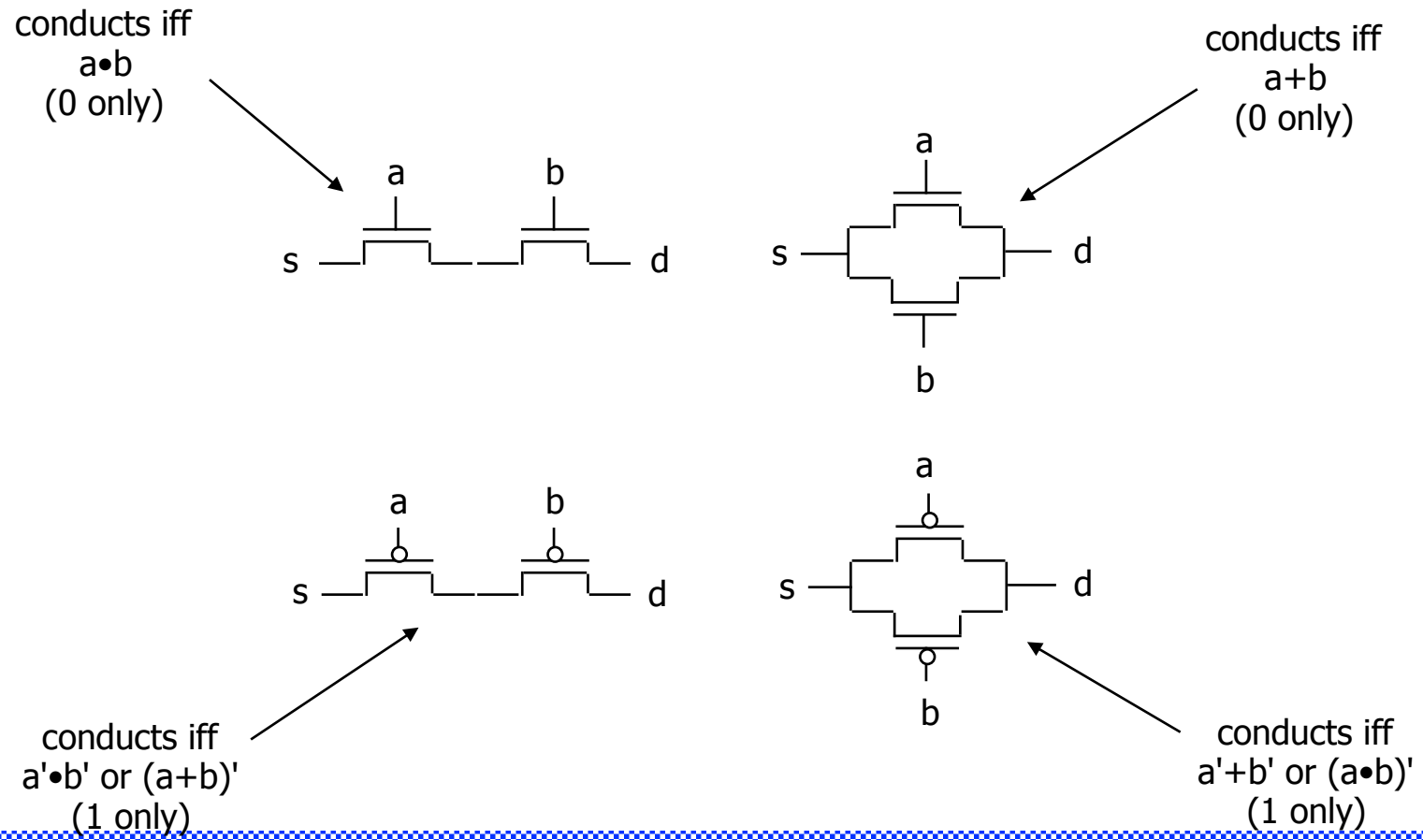


Transistors as Switches

- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain

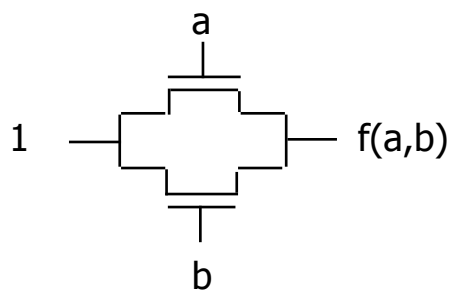


Switching Logic



Implementation of Logic Gates

- OR gate

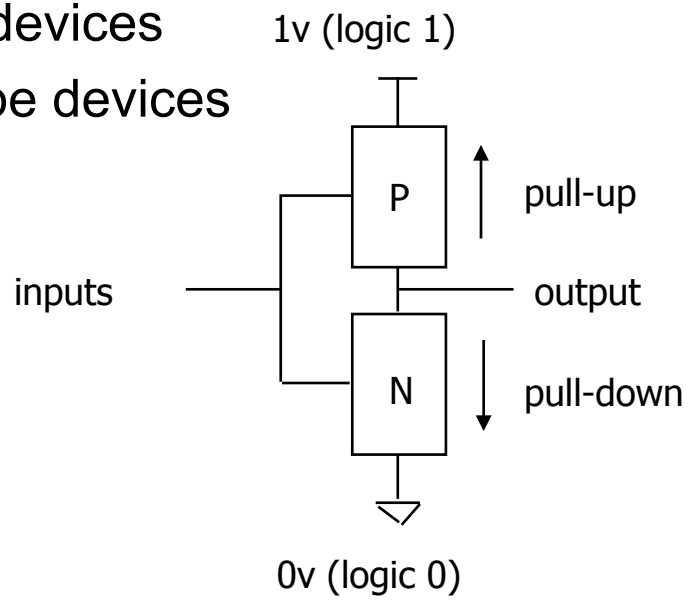


a	b	a + b
0	0	0
0	1	1
1	0	1
1	1	1

- Two problems
  - 1) when a=b=0, f(a,b) is undefined (floating)
  - 2) n- type switches do not conduct 1 well
- Two solutions
  - when f=0, connect output to 0v using n-type switches
  - when f=1, connect output to 1v using p-type switches

Complementary CMOS Gates

- Pull-up network consisting of p-type devices
- Pull-down network consisting of n-type devices

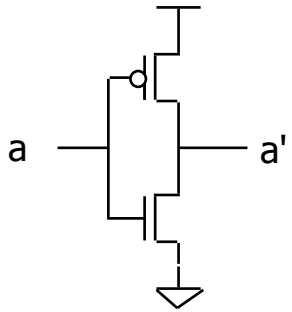


- Example: an inverter

a	a'
0	1
1	0

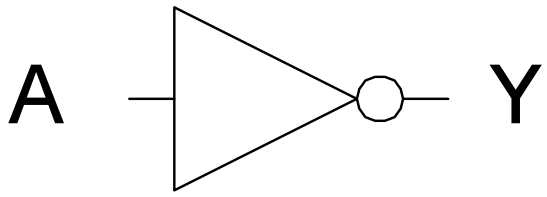
↑: a'

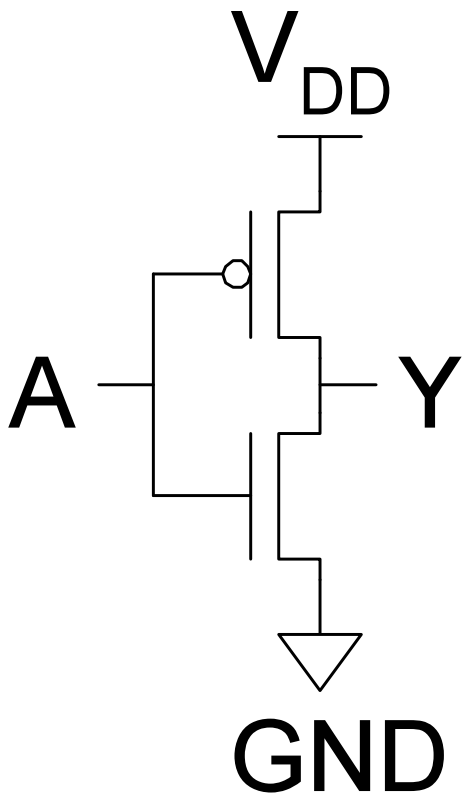
↓: a



CMOS Inverter

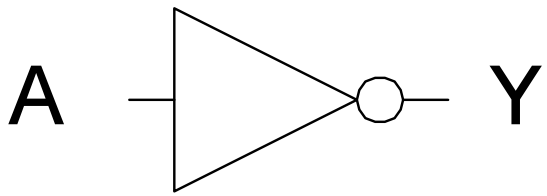
A	Y
0	
1	

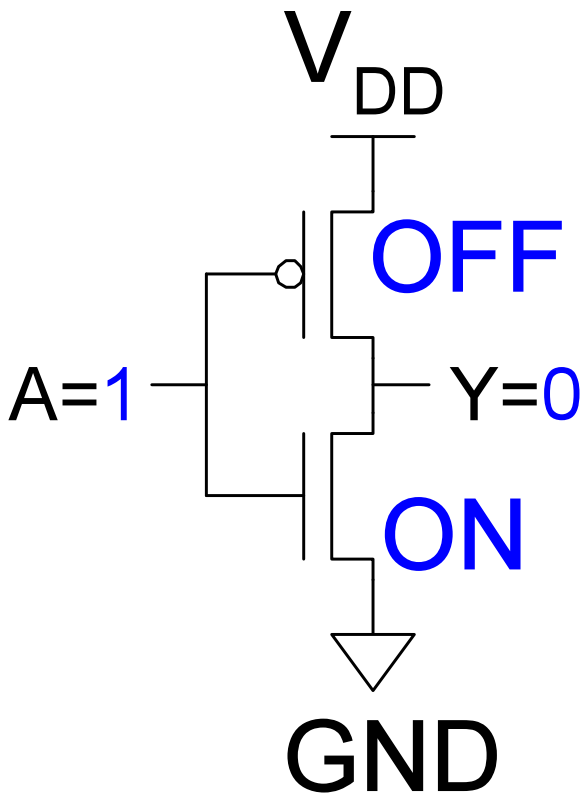




CMOS Inverter

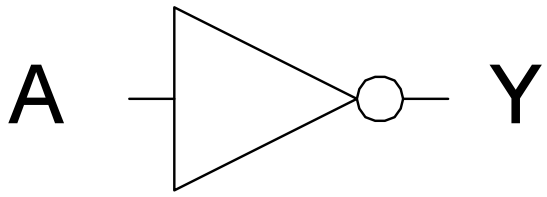
A	Y
0	
1	**0**

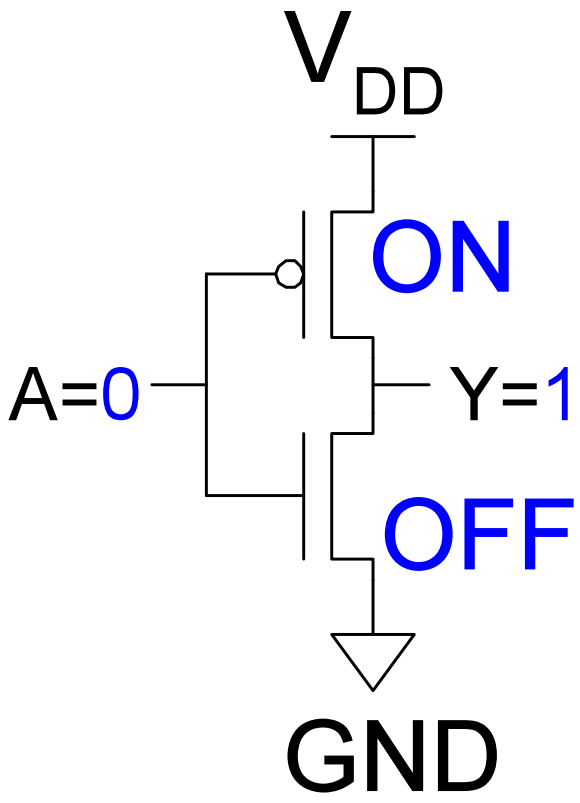




CMOS Inverter

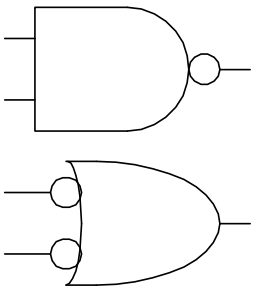
A	Y
0	**1**
1	0

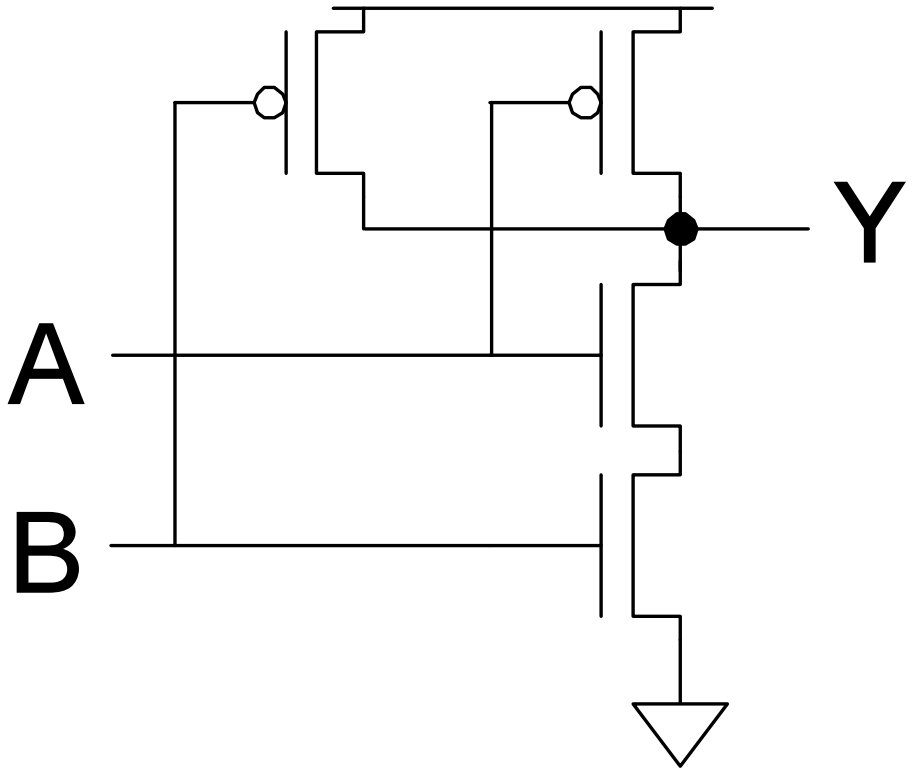




CMOS NAND Gate

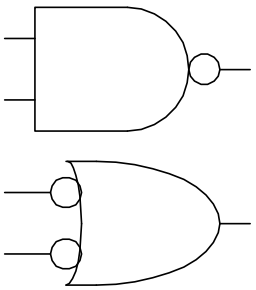
A	B	Y
0	0	
0	1	
1	0	
1	1	

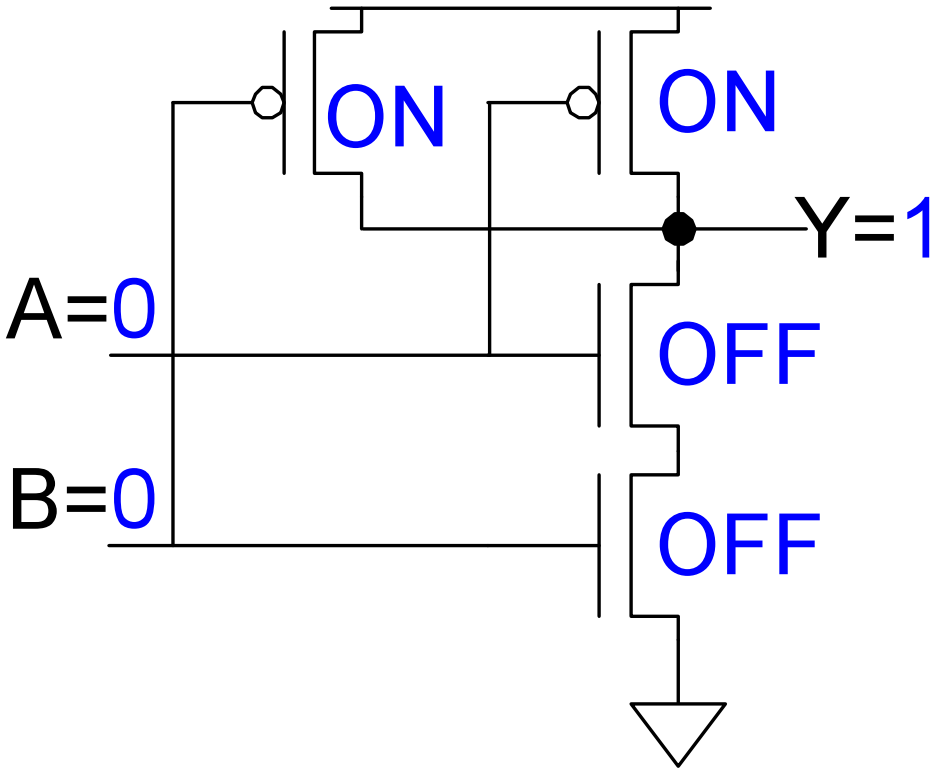




CMOS NAND Gate

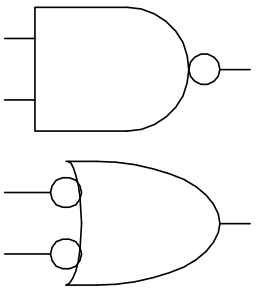
A	B	Y
0	**0**	**1**
0	1	
1	0	
1	1	

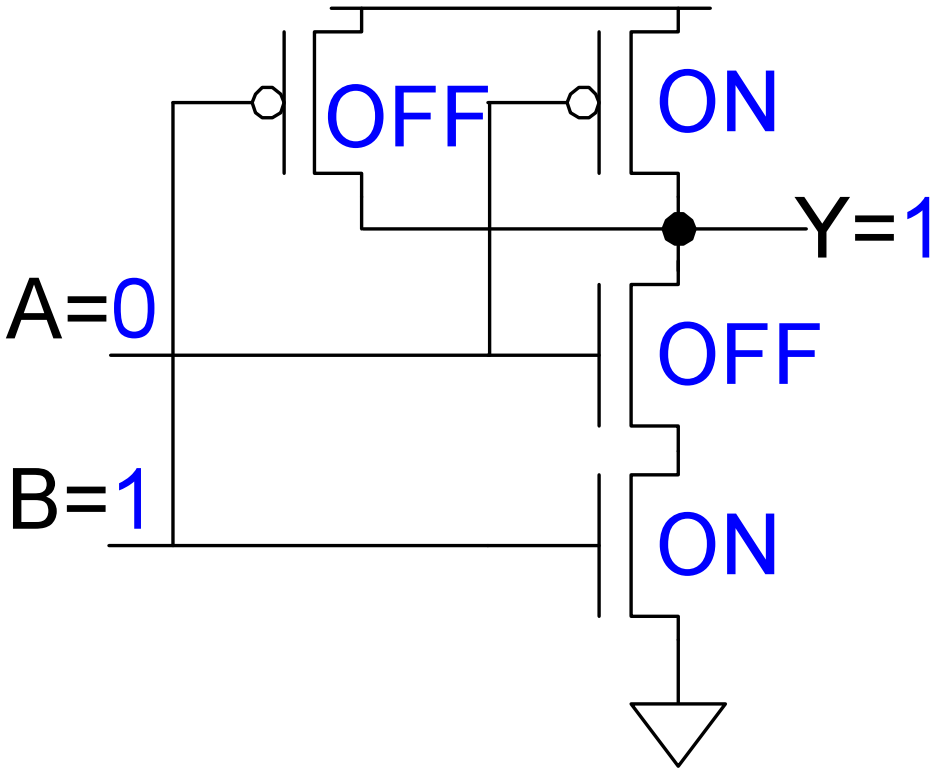




CMOS NAND Gate

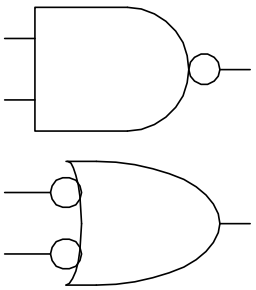
A	B	Y
0	0	1
0	**1**	**1**
1	0	
1	1	

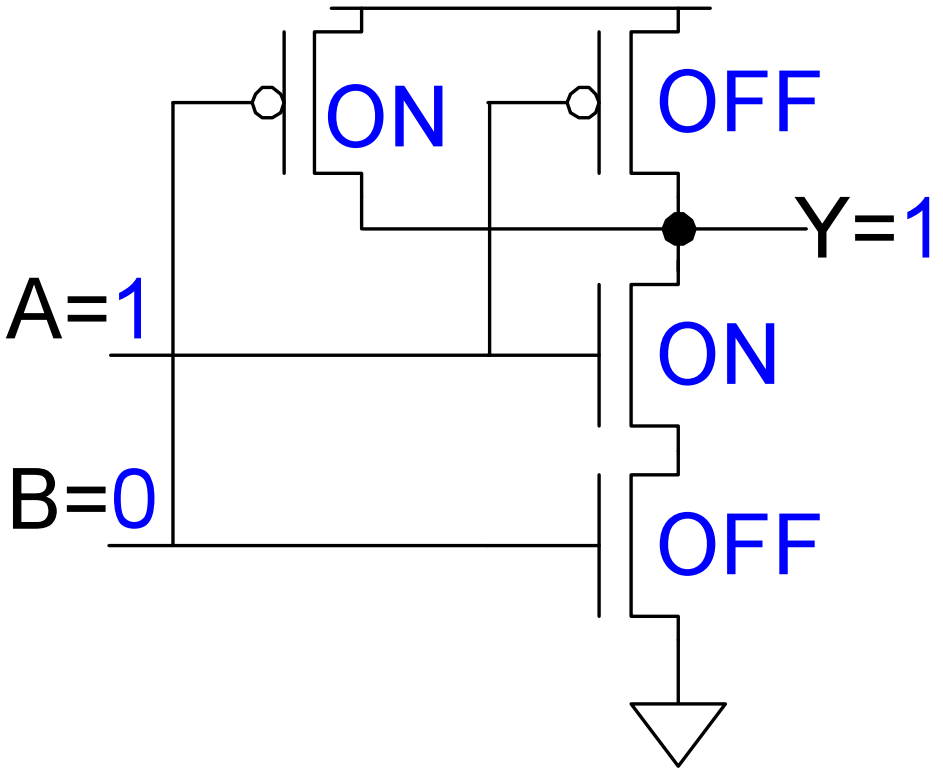




CMOS NAND Gate

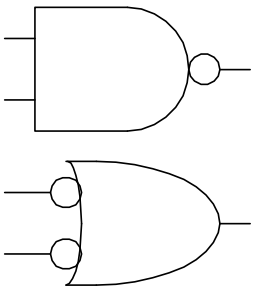
A	B	Y
0	0	1
0	1	1
1	**0**	**1**
1	1	

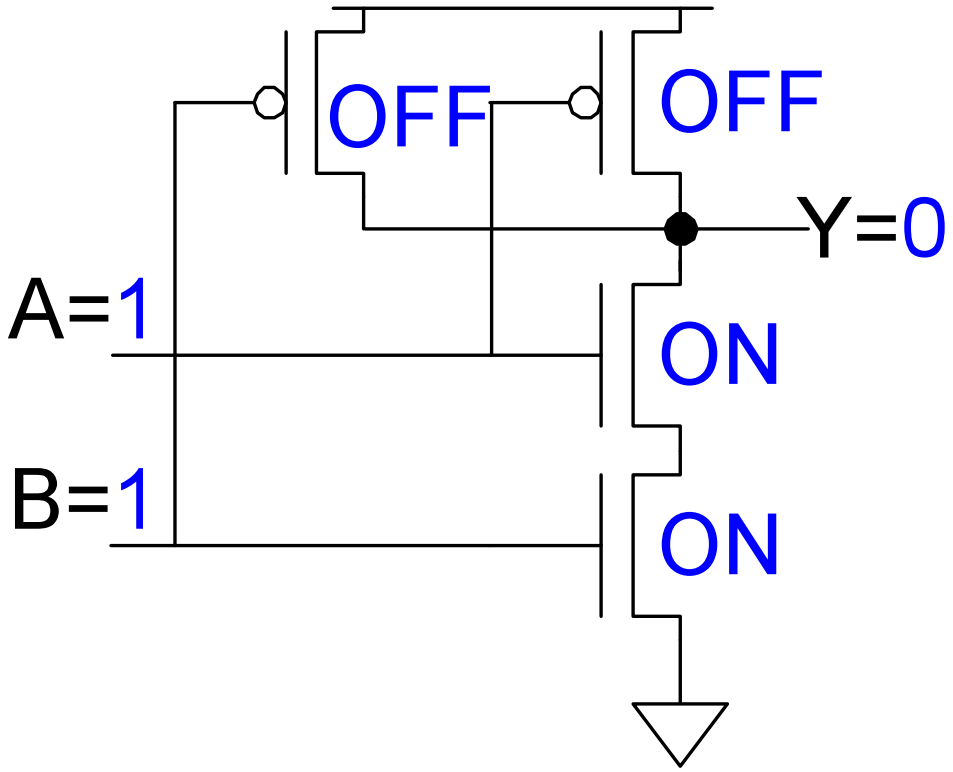




CMOS NAND Gate

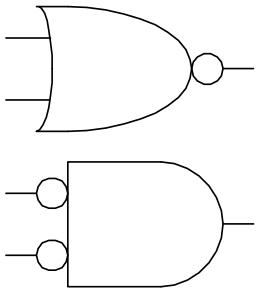
A	B	Y
0	0	1
0	1	1
1	0	1
1	**1**	**0**

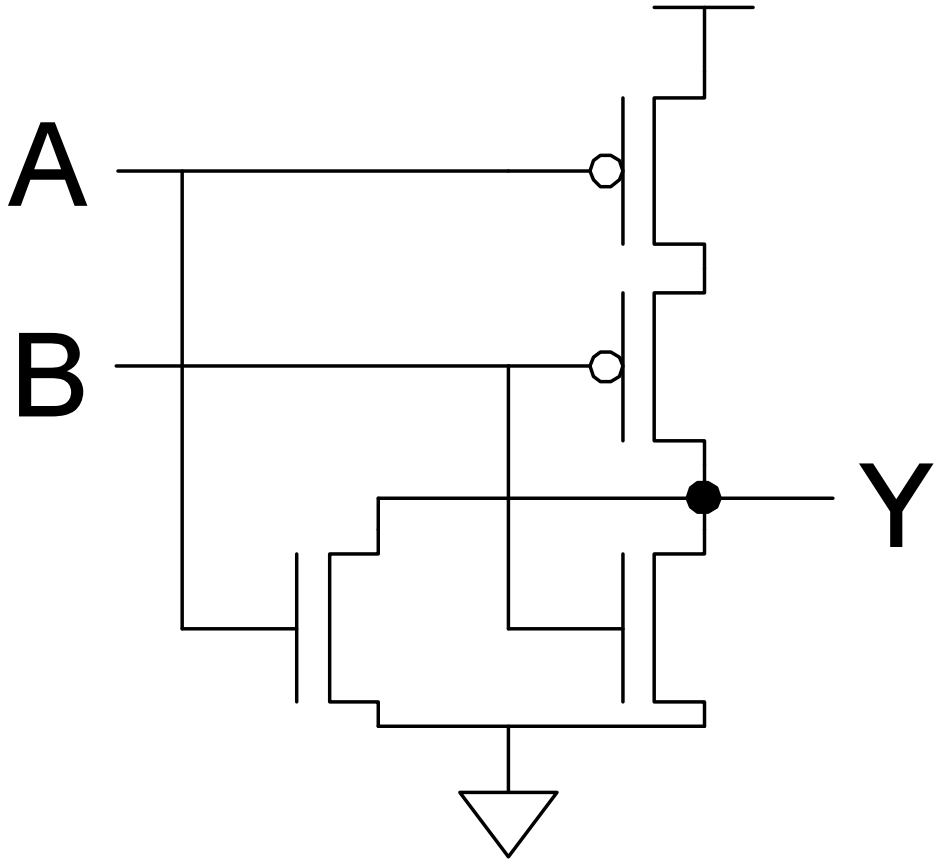




CMOS NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



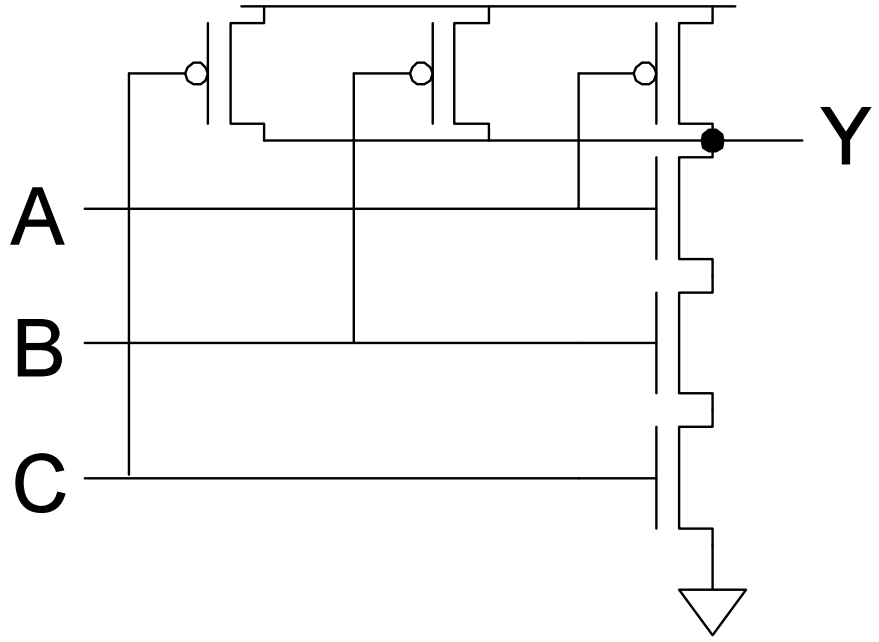


3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

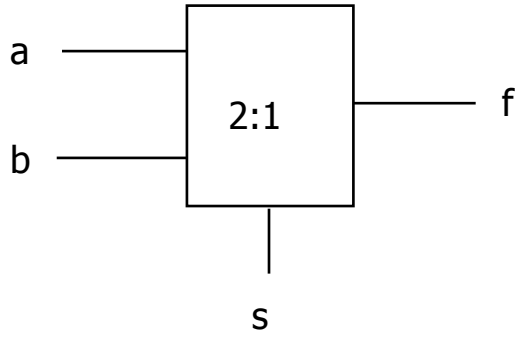
3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0



Switch Logic vs. Gate Logic

- Example: two-input multiplexer



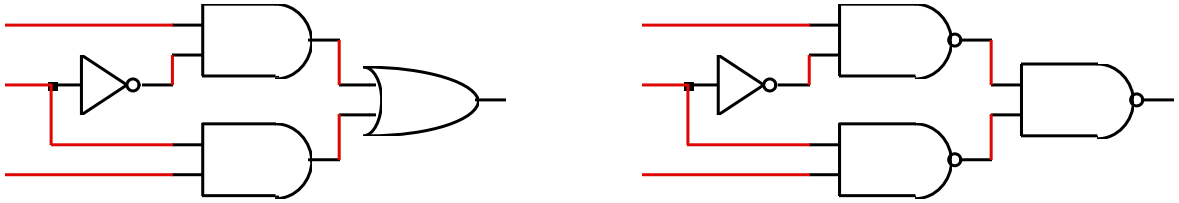
f=a, when s=0

f=b, when s=1

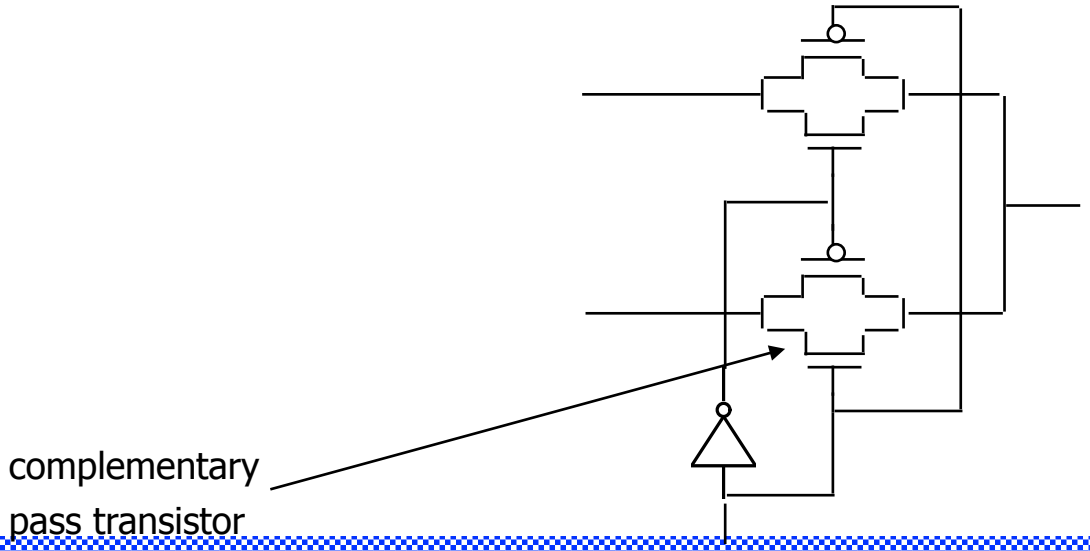
f=s'a+sb

Switch Logic vs. Gate Logic

- Two-input mux with gate logic (14 transistors)

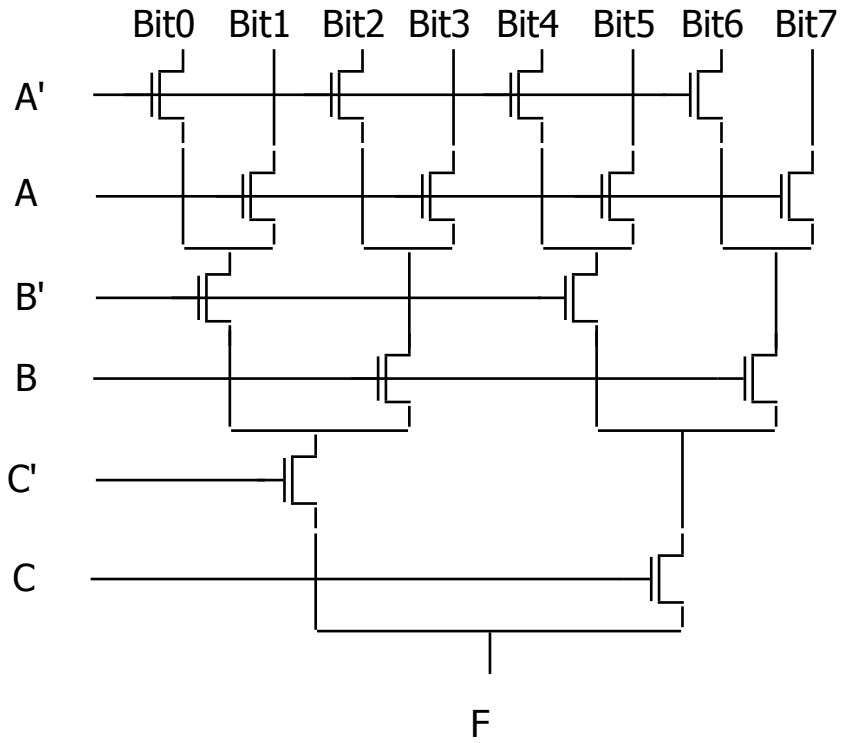


- Two-input mux with switch logic (6 transistors)



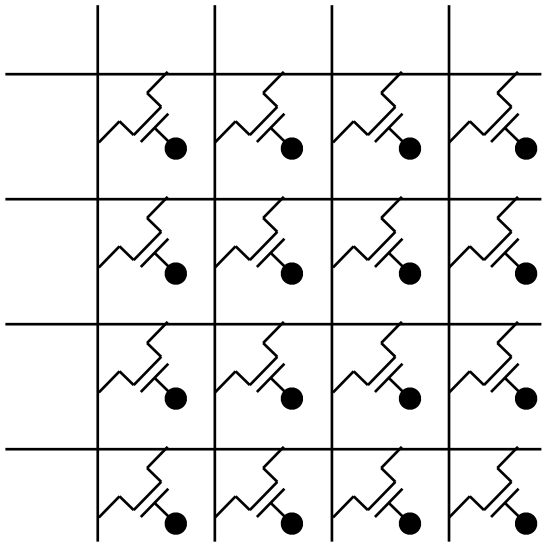
Implementing LUTs

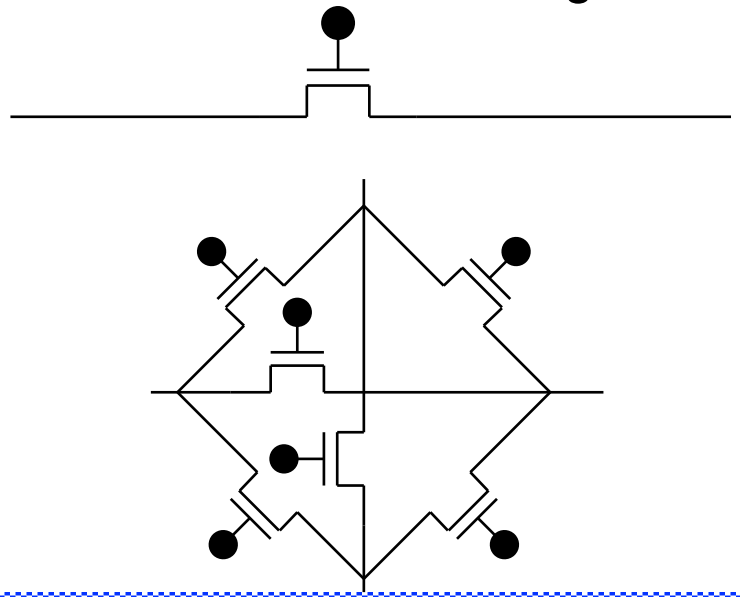
- Multiplexor logic – simple switch network (a tree)
  - inputs: programming bits
  - controls: inputs to CLB
  - output: function value
- However, series transistors are slow – $O(n^2)$



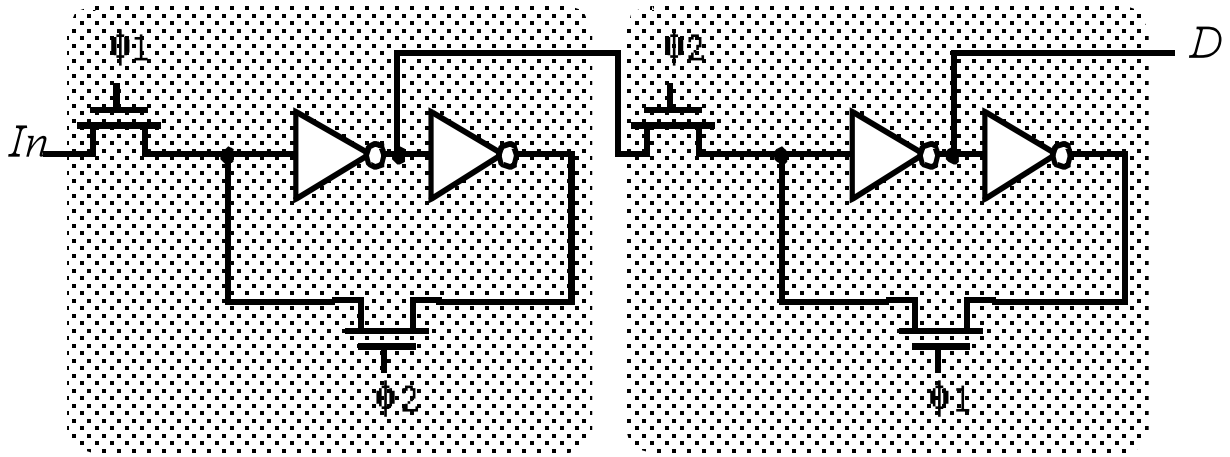
Programmable Interconnect

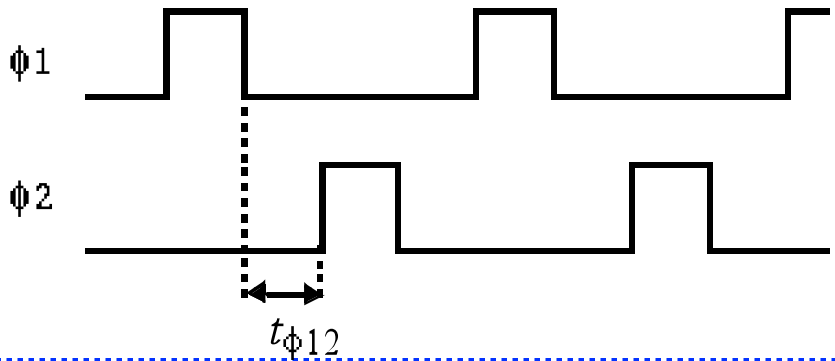
- Switches connect wires at intersections
- Can also be used to segment wire
- Repeaters needed every so often
  - simple non-inverting buffers (2 inverters)
  - otherwise, too many switches in series slow down signal



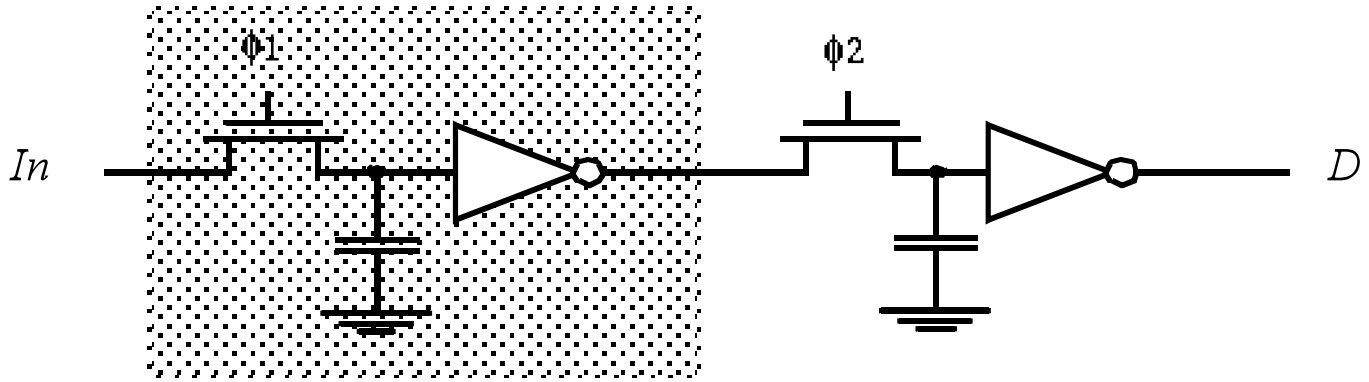


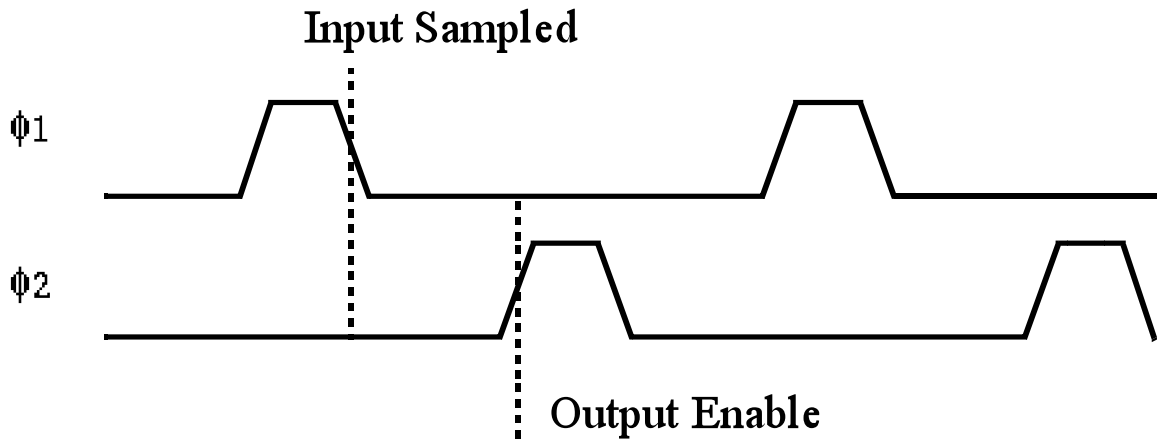
Master-Slave Register





Dynamic Register

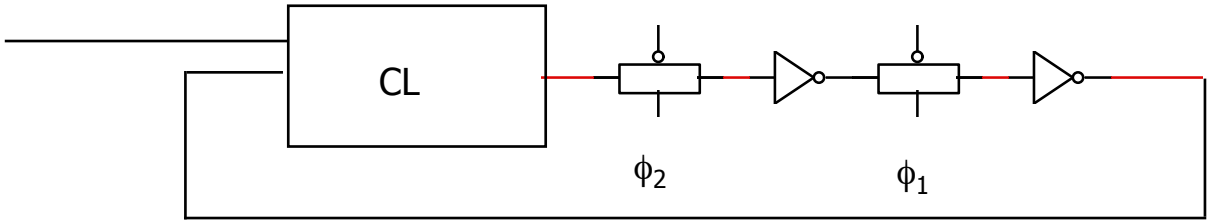




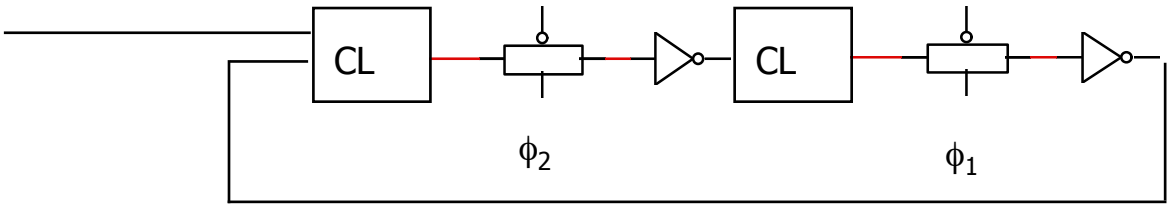
Latch-Based Design

- Switches and/or gates compute new values to store on next clock cycle

straightforward implementation

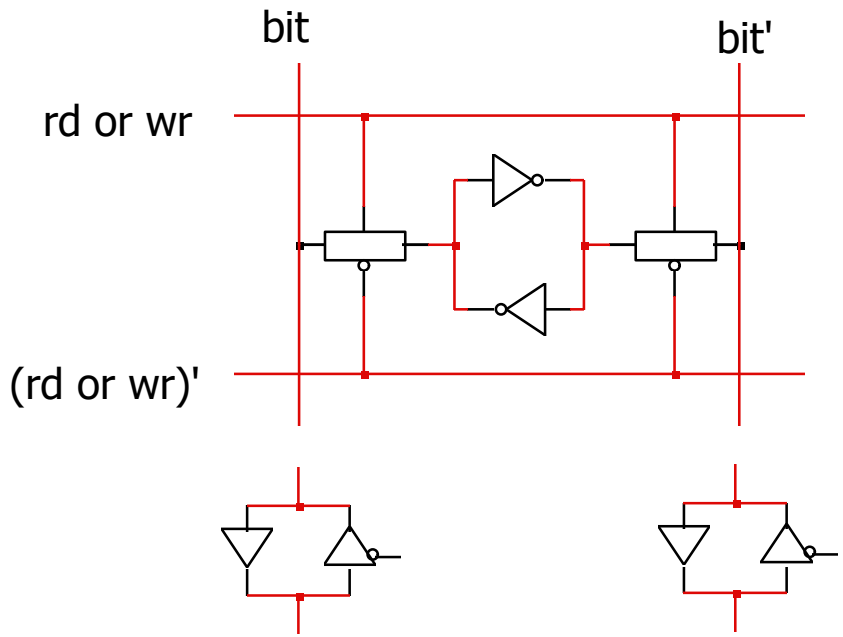


this circuit can use the entire clock cycle – no wasted time - a form of retiming



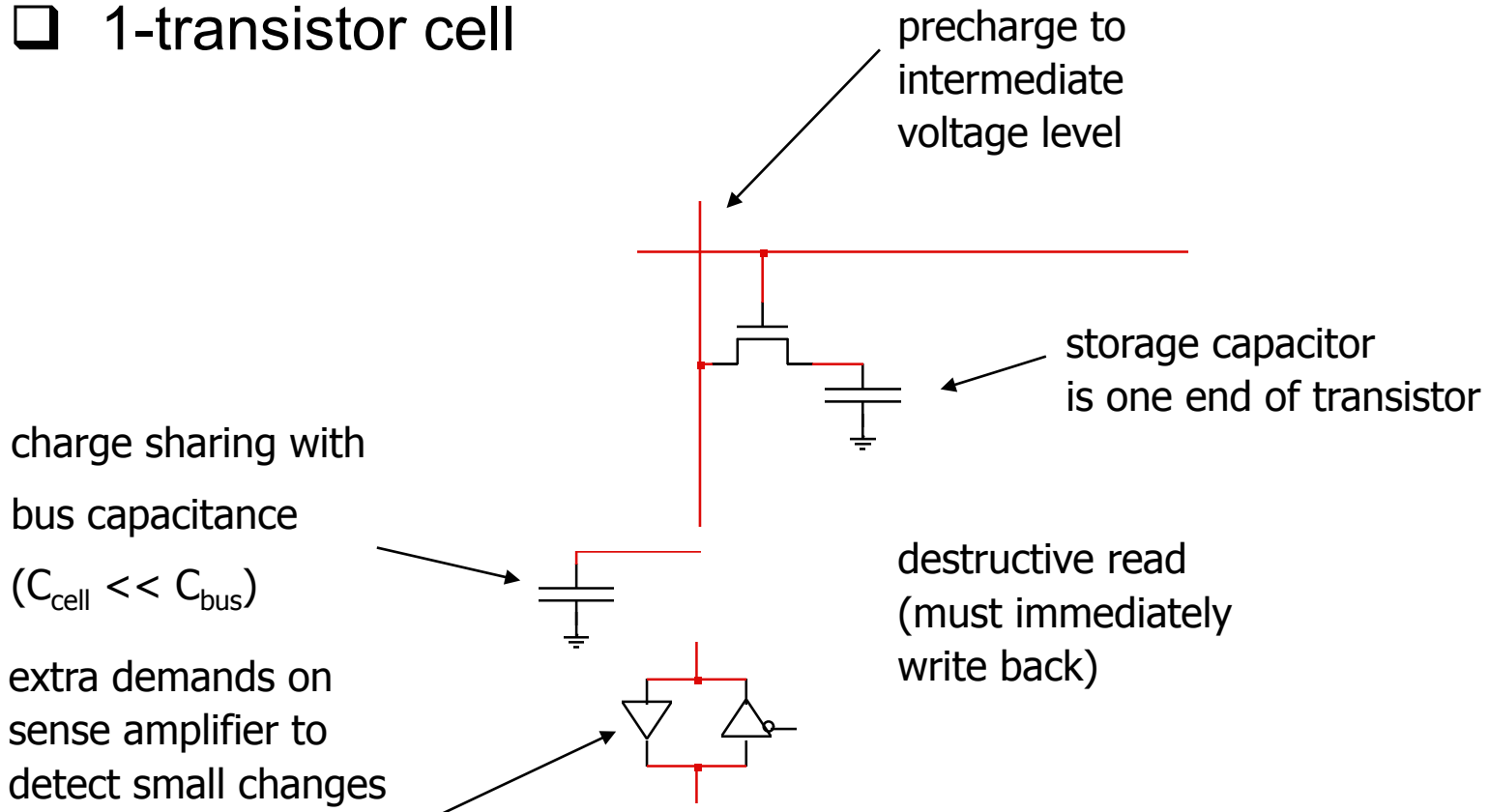
Static Memory Cell

- 8-transistor cell
- N-transistor only: 6T cell



Dynamic Memory Cell

- 1-transistor cell

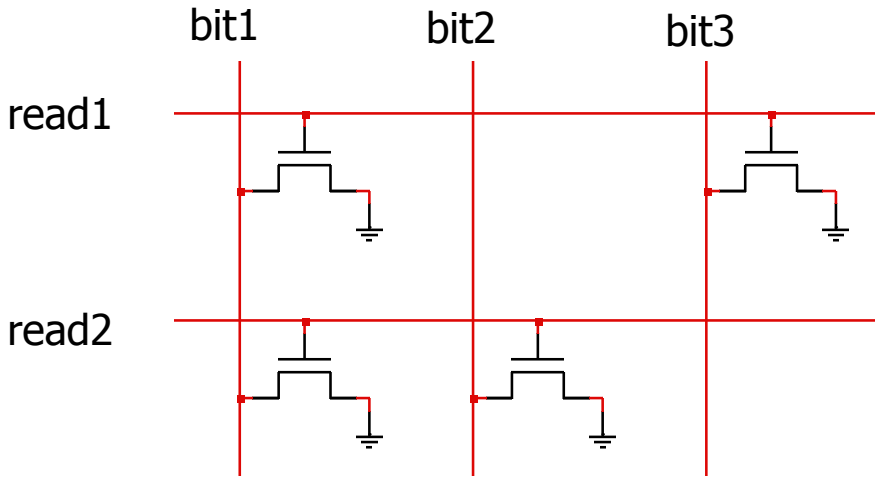


Dynamic storage

- Capacitor implemented by gate capacitance of transistor
- No capacitor is perfect
  - charge leaks away through imperfect switches
- Must be replenished or refreshed
  - 'memory' lasts about 1ms
- Solution: periodically read the value and write it back

Read-only Memory Cells

- To store constants or other invariant data
- Popular for control implementation

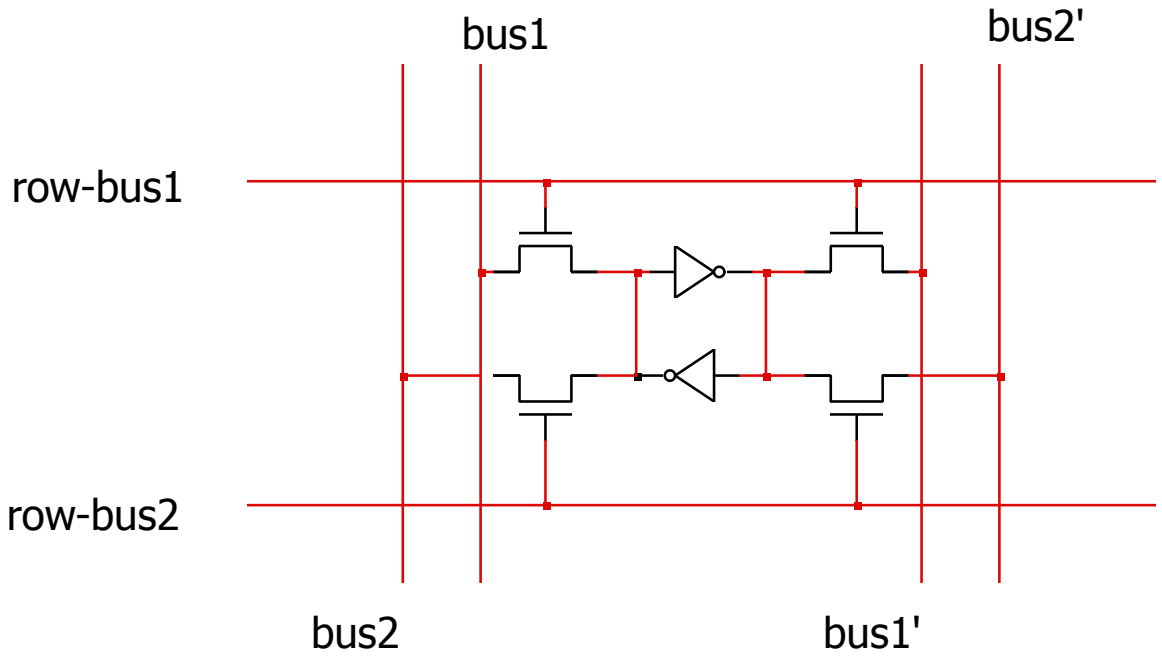


programmable logic array structure

(exploits distributed NOR gate structure)

Multi-ported Register Cells

- Augment 6T cell for more I/O

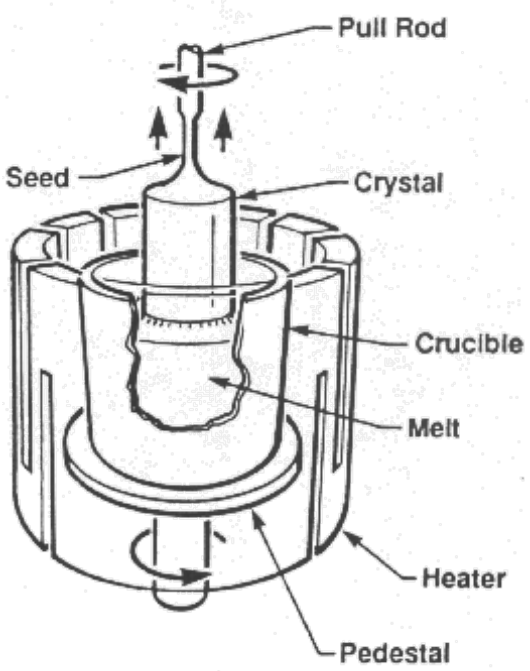


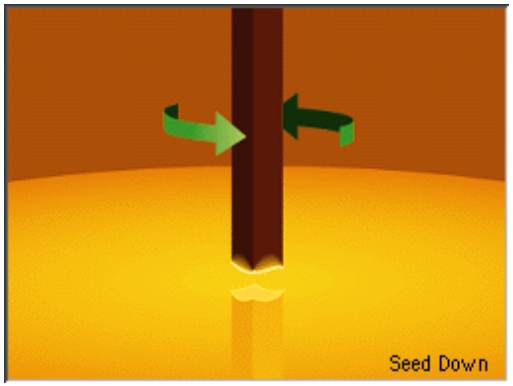
CMOS Fabrication

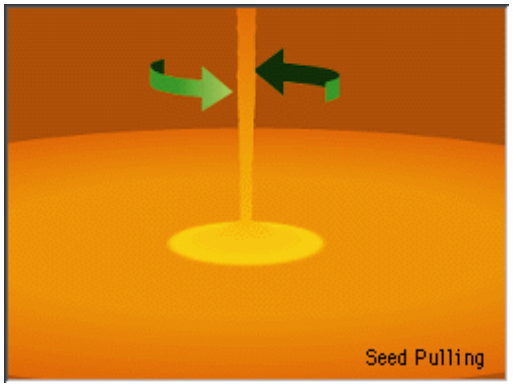
- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

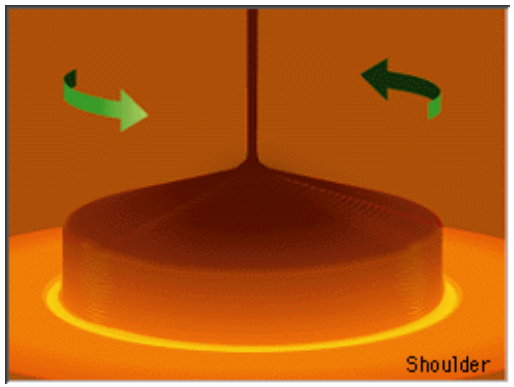
The wafer

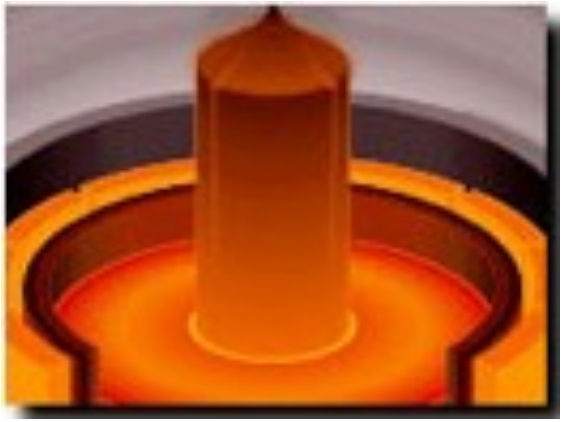
- Czochralski process
  - Melt silicon at 1425 °C
  - Add impurities (dopants)
  - Spin and pull crystal
- Slice into wafers
  - 0.25mm to 1.0mm thick
- Polish one side




Seed Down

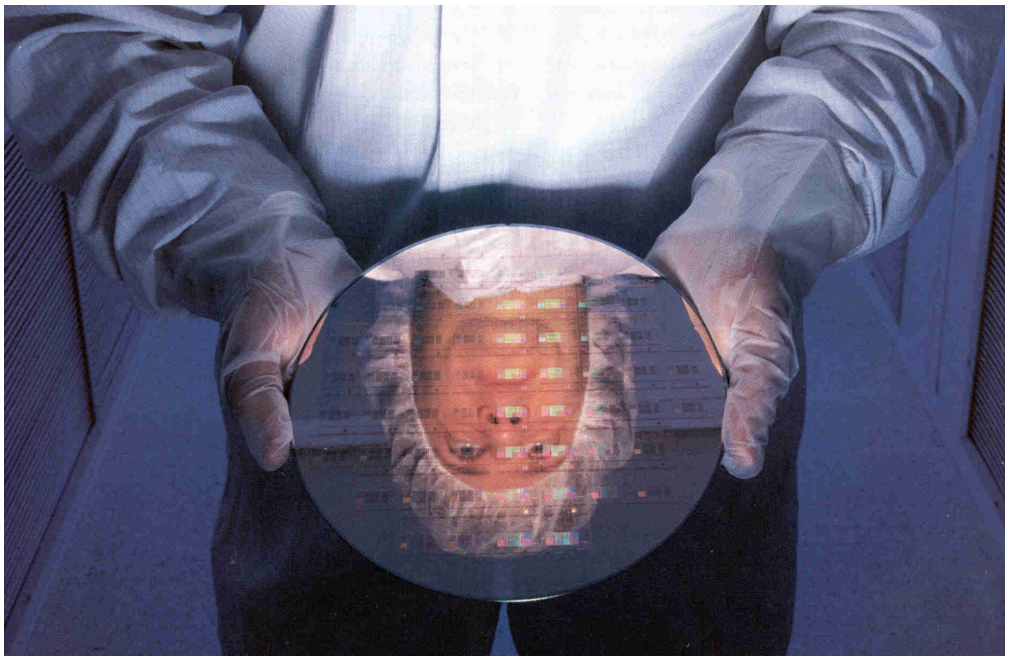

Seed Pulling


Shoulder



Crystal and wafer

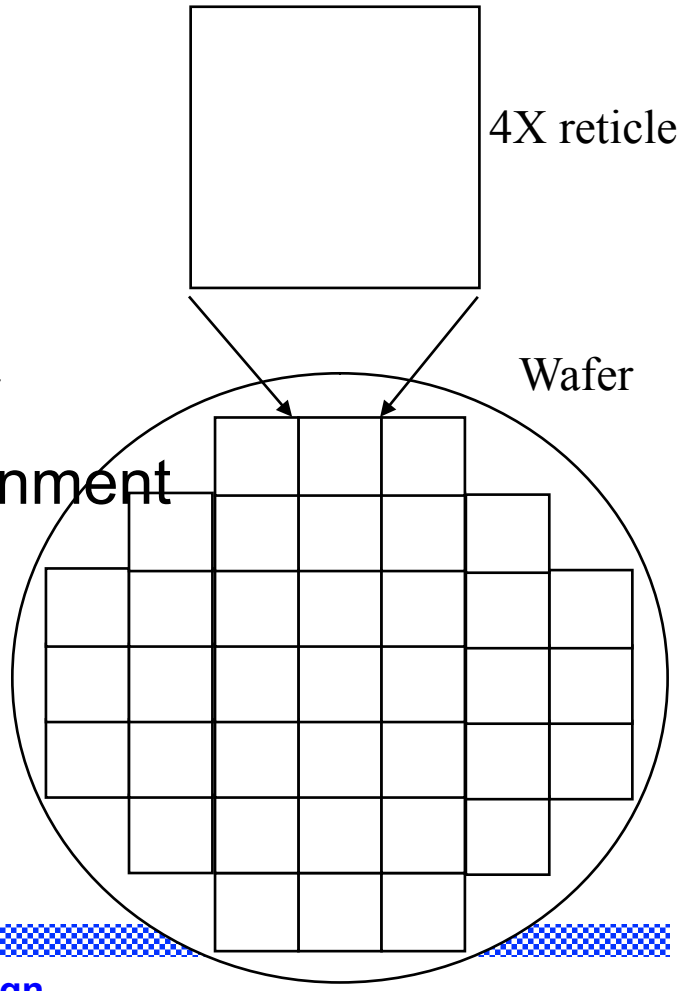
Wand
(a finished 250lb crystal)



A polished wafer

The mask

- Illuminate reticle on wafer
  - Typically 4× reduction
- Typical image is 25×25mm
  - Limited by focus
- Step-and repeat across wafer
  - Limited by mechanical alignment



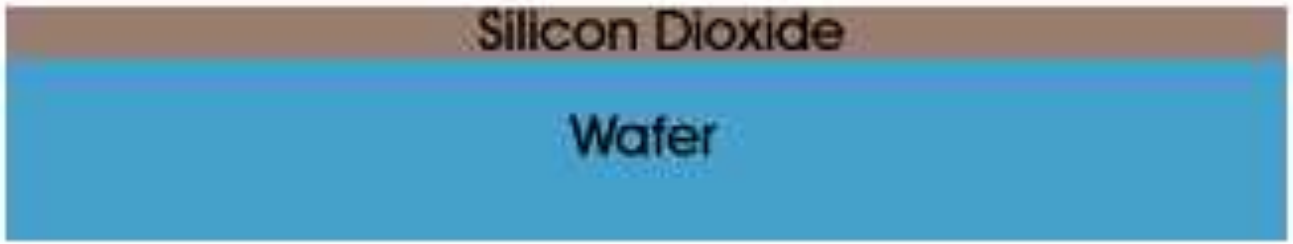
Lithography

- Patterning is done by exposing photoresist with light
- Requires many steps per “layer”

- Example: Implant layer

Reference: FULLMAN KINETICS

Grow Oxide Layer

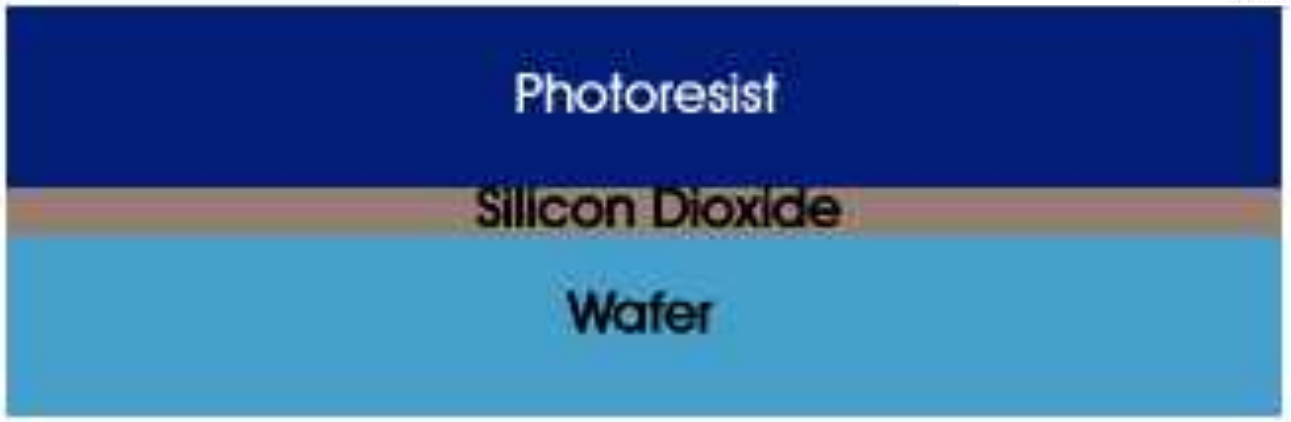


Oxidation Layering

Reference: FULLMAN KINETICS

Add Photoresist

Photoresist Application
(Ontrak)

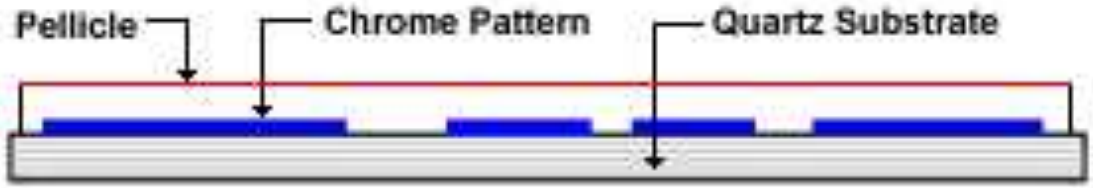


Photoresist Coating

Reference: FULLMAN KINETICS

Mask

Pattern
Preparation

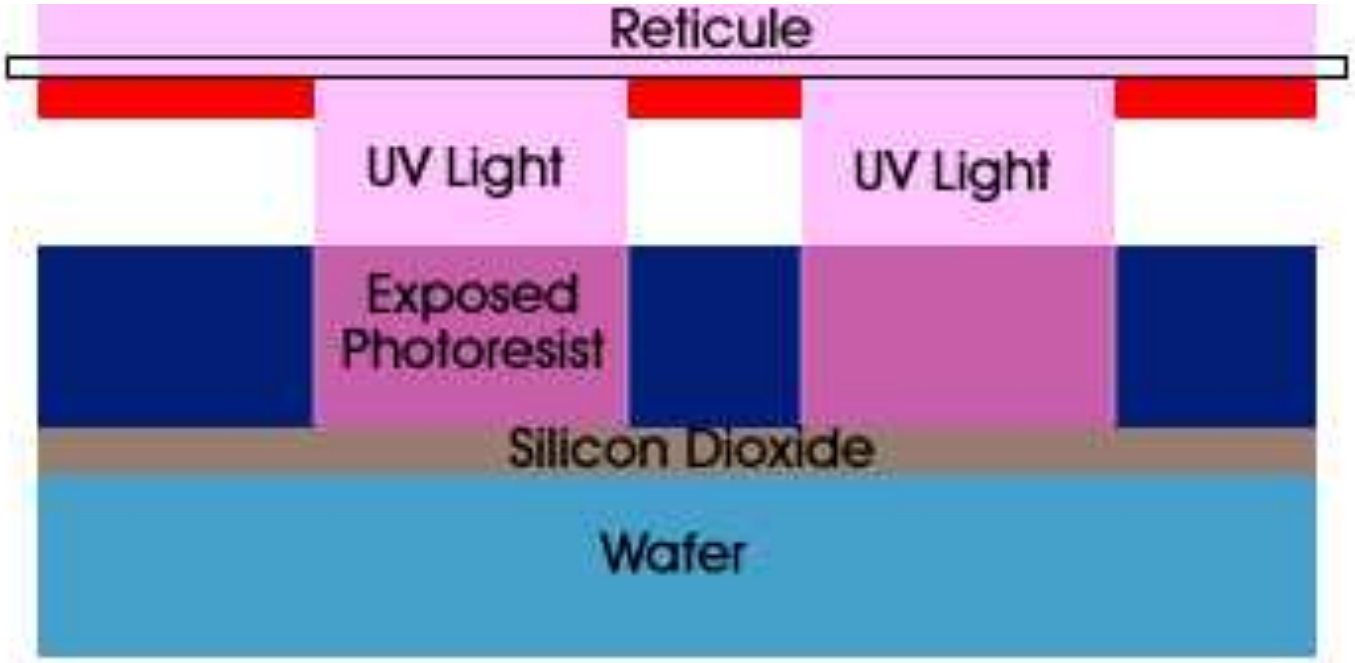


Reticle

Pattern Preparation

Reference: FULLMAN KINETICS

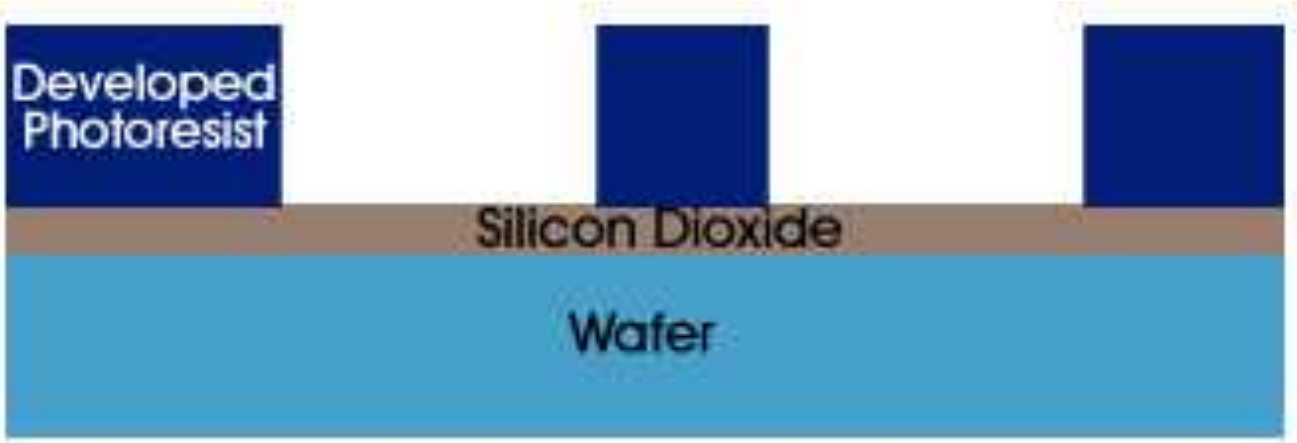
Expose using UV Light



Photolithography

Reference: FULLMAN KINETICS

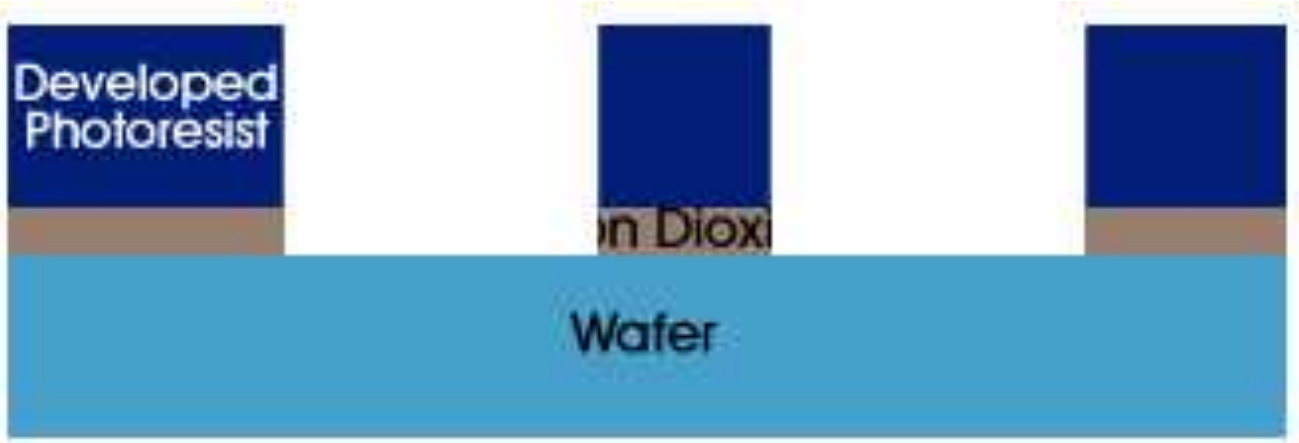
Develop and Remove Resist



Photoresist Developing

Reference: FULLMAN KINETICS

Etch Silicon Dioxide



Dielectrics Etching

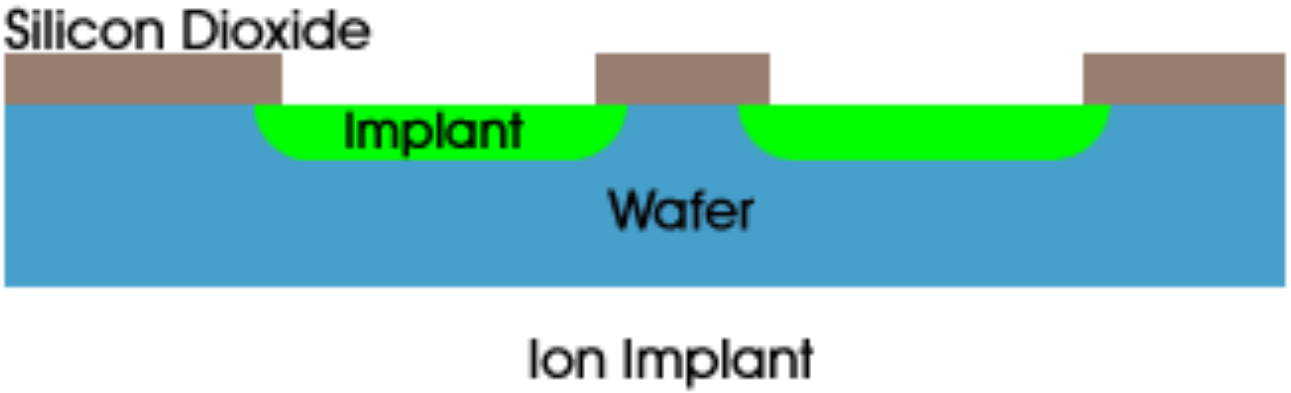
Reference: FULLMAN KINETICS

Remove Resist

Photoresist Ashing

Reference: FULLMAN KINETICS

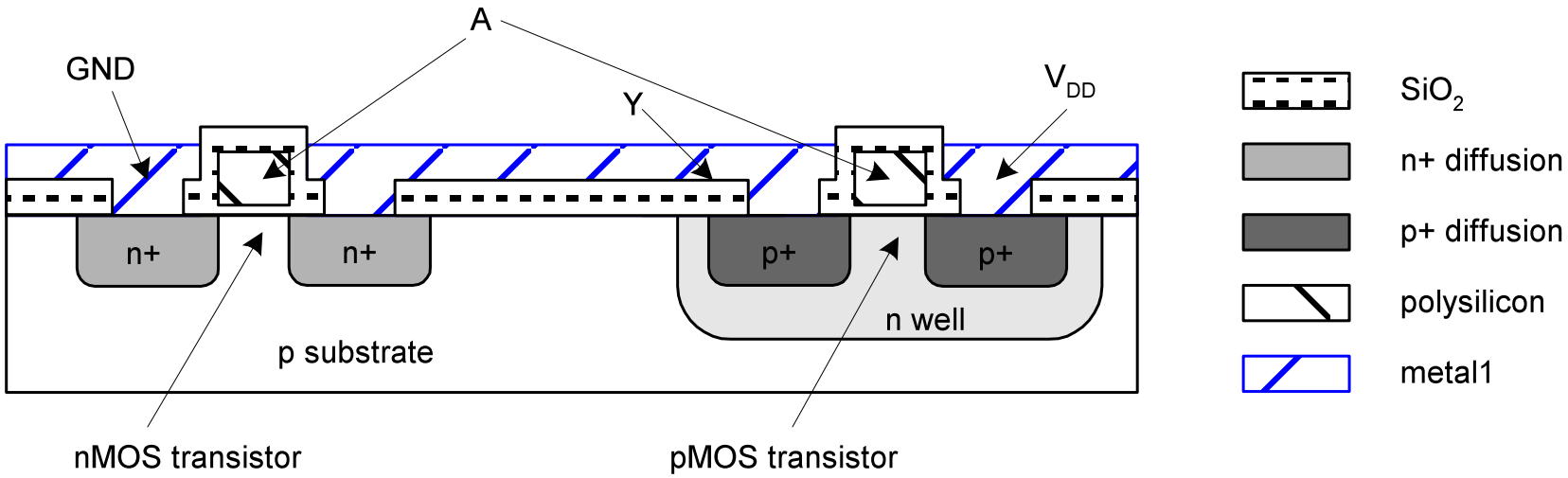
Implant Dopant



Reference: FULLMAN KINETICS

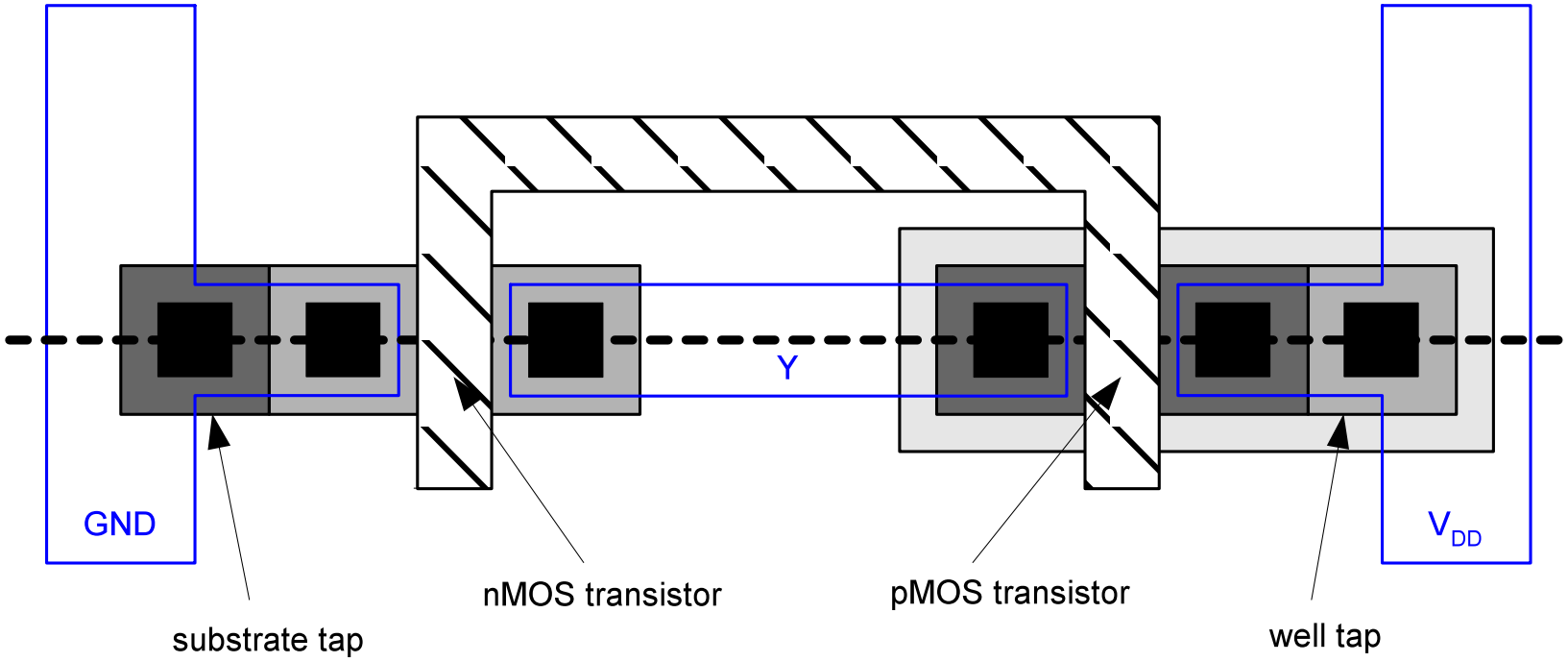
Inverter Cross-section

- Typically use p-type substrate for nMOS transistor
  - Requires n-well for body of pMOS transistors
  - Several alternatives: SOI, twin-tub, etc.

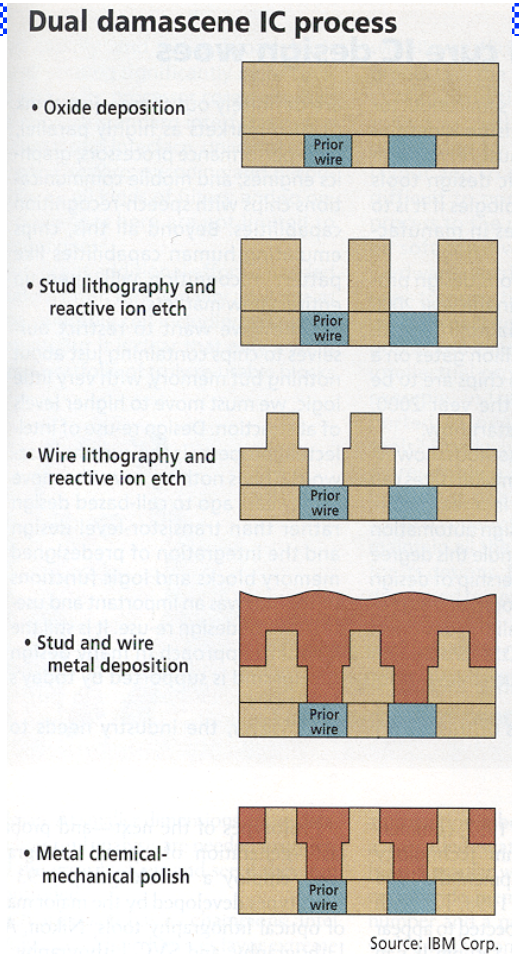


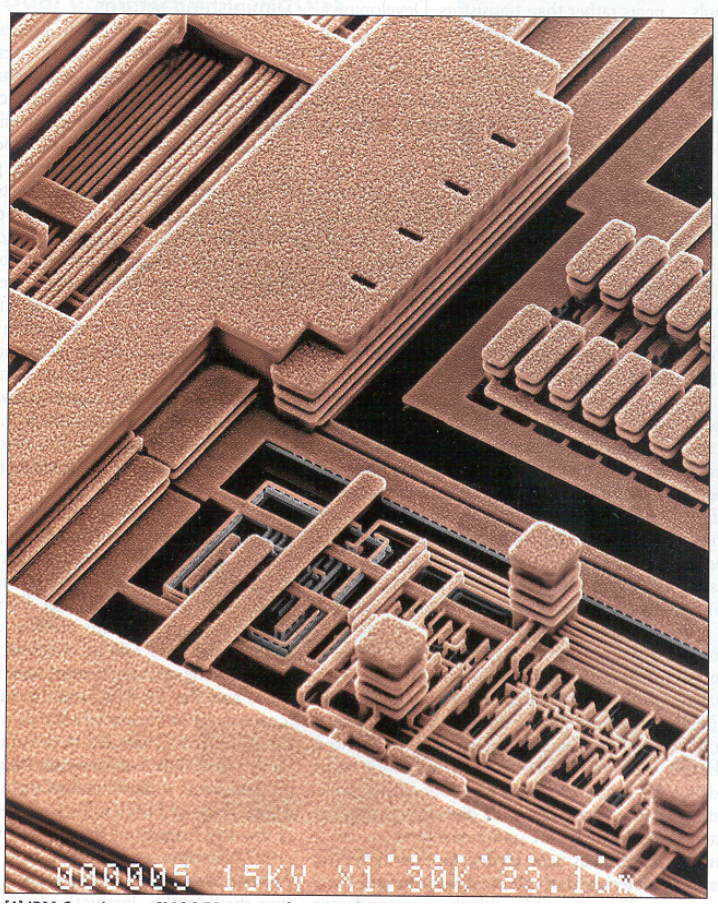
Inverter Layout

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Advanced Metallization - Copper



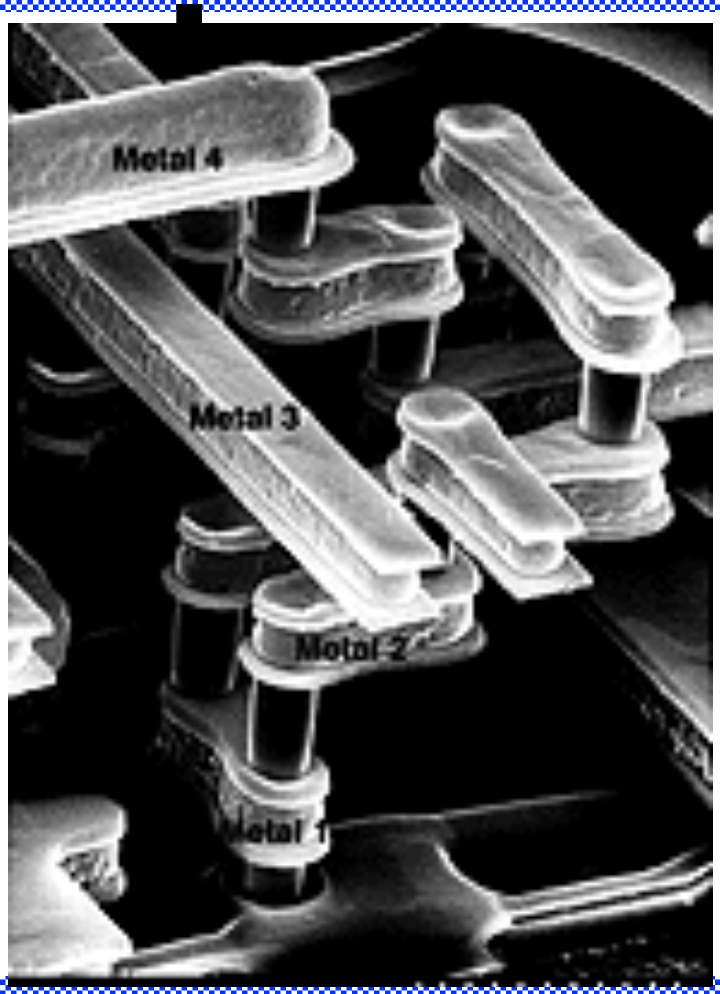


Copper versus Aluminum

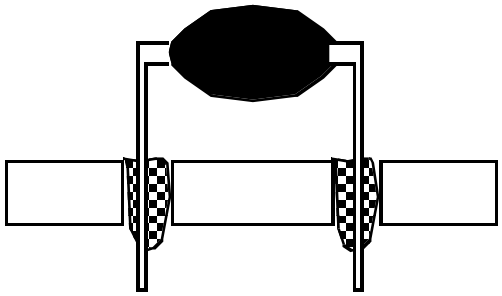
~ 40% lower resistivity

~ 10× less electromigration

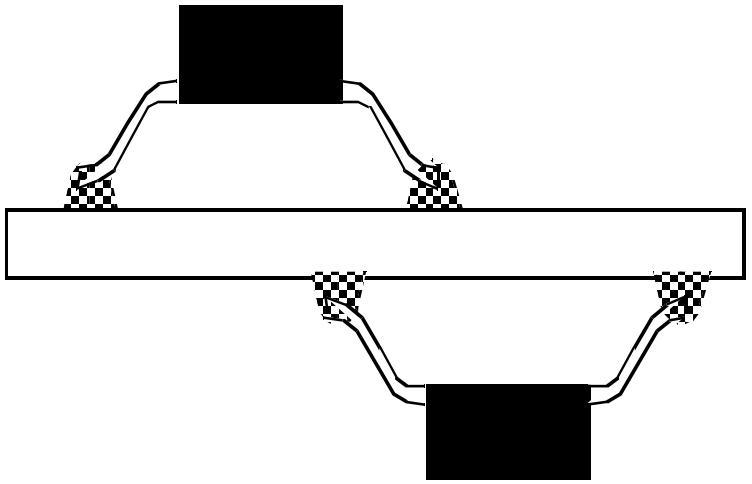
A View of Interconnect



Package-to-Board Interconnect

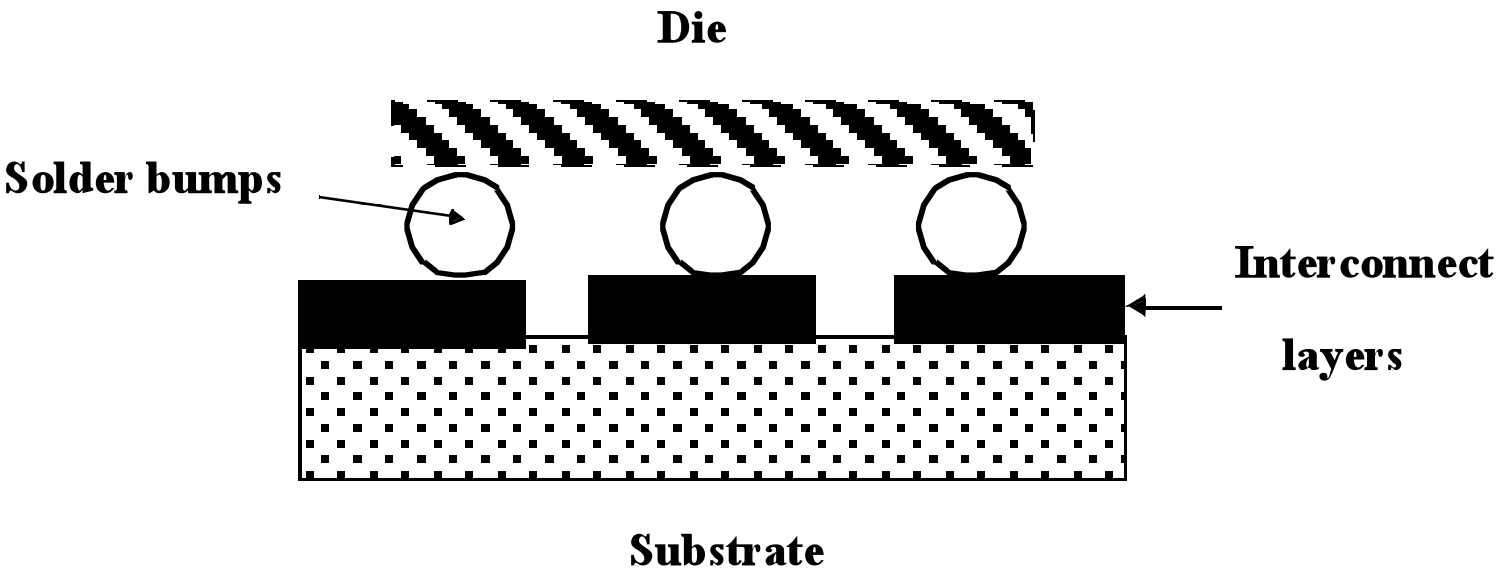


(a) Through-Hole Mounting

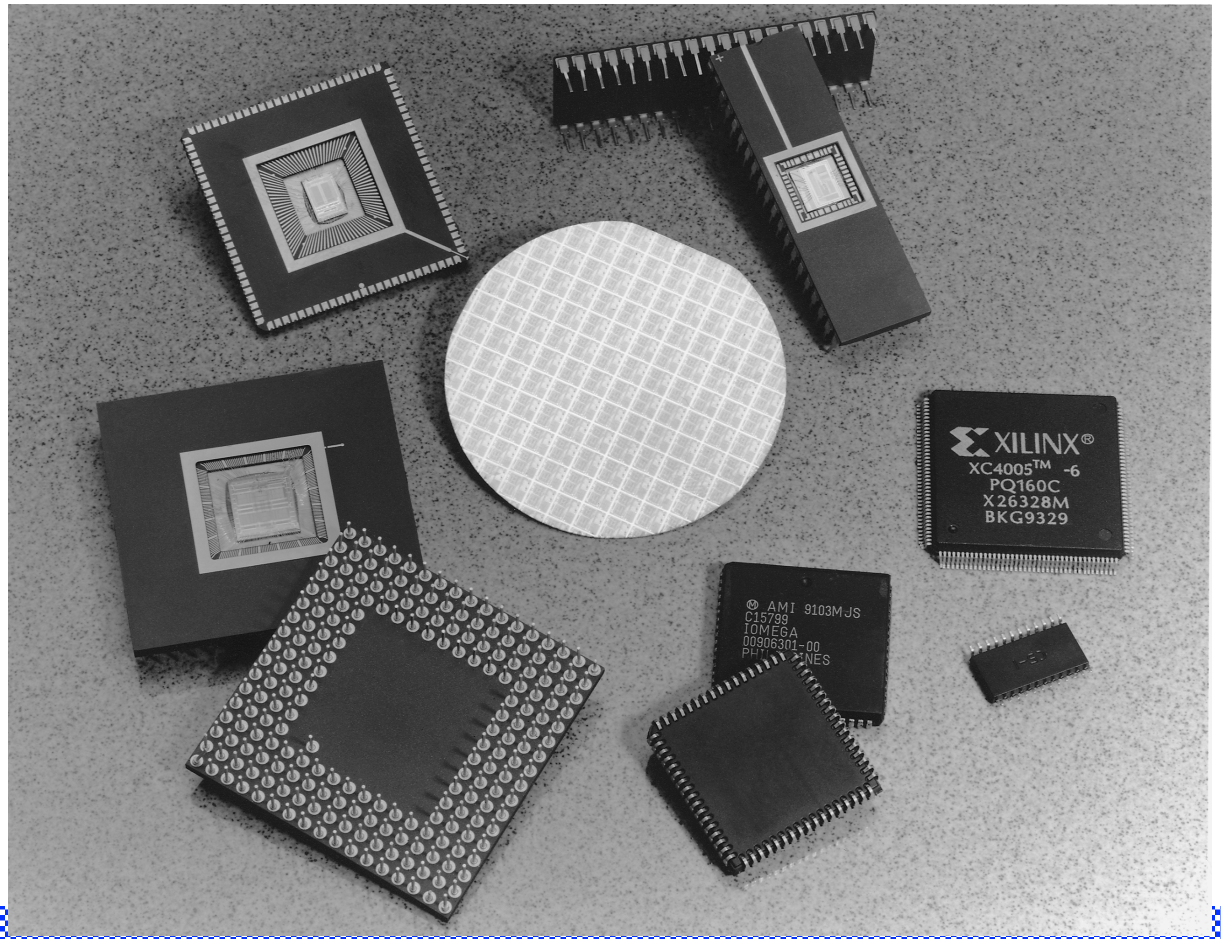


(b) Surface Mount

Flip-Chip Bonding



Package Types



Multi-Chip Modules