1. The circuit in Figure 1 adds two 32-bit numbers by chaining two 16-bit adders. Given the delay characteristics of the circuit elements given below, what is the maximum clock frequency we can use assuming zero clock skew?

   **Register:** \( t_{pd} = [200, 300] \text{ ps}, \ t_{su} = 200 \text{ ps}, \ t_{h} = 100 \text{ ps} \)

   **Adder:** \( t_{pd} = [200, 800] \text{ ps} \)

   Note: \([\text{min}, \text{max}]\) gives the minimum and maximum propagation delay

2. Let’s assume that the clock skew can be up to 400ps. between any two registers, positive or negative. Does the circuit still work? Why not?

3. What can you do to make the circuit work with this amount of clock skew? (Assume that you have a buffer with delay \([100, 200]\) ps that you can insert anywhere in the circuit if you need it.)

4. How can you speed up this circuit by pipelining? Assuming a more reasonable clock skew of only 200ps, how fast can you operate the pipelined circuit?

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**Figure 1**

- The circuit in Figure 1 adds two 32-bit numbers by chaining two 16-bit adders.
5. Figure 2 shows an asynchronous interface that delivers 8 bits of data every dclk cycle. The sender is designed so that the rising edge of dclk is centered between the times where data changes to negate the effect of skew. That is, there is always some difference in the delay of the wires between the sender and the receiver. If this difference (skew) can be as much as 2ns, what is the minimum clock period for dclk and what determines it? Use the following register timing characteristics:

Register: \( t_{pd} = [200, 300] \) ps, \( t_{su} = 200 \) ps, \( t_h = 100 \) ps

6. Design a circuit that synchronizes the data input, which is in the dclk clock domain, to the clk clock domain. This circuit should assert the register clock enable so that each new input data is clocked into the register reliably. (Note that this clock enable signal is also used to indicate that new valid data has been latched.) Show that your circuit works if the system clock runs at 100MHz, and dclk runs at 25MHz.

7. Presumably your circuit in problem 5 used a “synchronizer” circuit consisting of back-to-back registers to cross the clock boundary. Calculate the MTBF for your circuit given register characteristics of \( \tau = 300 \) ps and \( T_0 = 2 \mu \) sec. Let’s say you are not satisfied with this. What are the two primary ways to improve the reliability of this circuit? What are the system implications of each?

8. [Extra credit] Let’s increase dclk to 40MHz. Does your circuit from # 6 still work? How can you change it to work? What happens to the MTBF?