HPS, A NEW MICROARCHITECTURE: RATIONALE AND INTRODUCTION
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HPS (High Performance Substrate)

• A Micro-architecture for High Performance Computing

• Restricted Data Flow
  – Only a small subset of the entire program is in the HPS micro-engine at any one time
    • Active window
Abstract view of HPS

Static I-Stream

Branch Predictor

Dynamic I-Stream

Active window

Decoder/Merger

Tables

Value Buffer

Fetch Control

Retirement system

Data flow

Nodes in Tables awaiting firing

Issue

Fire

F.U F.U F.U

Dist

http://pplab.snu.ac.kr/courses/pa03/notes/HPS.ppt
Global data path of HPS

- Memory Alias Table
- Memory Staging Unit
- Merger
- Register Alias Table
- Result Buffer
- Note table
- Result Buffer
- Function Unit
- Memory System
- Memory Write Alias Table

From decoder

http://pplab.snu.ac.kr/courses/pa03/notes/HPS.ppt
An Example From the VAX

```
ADDIJ #1000, A, B
```

Diagram:

```
<table>
<thead>
<tr>
<th>READ</th>
<th>1</th>
<th>0</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>WRITE</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
```

```
1000 + Add A + Add B
```

```
WR
```

```
MKCER
```
Three kinds of Dependencies

• Data Dependency (RAW)
• Anti Dependency (WAR)
• Output Dependency (WAW)
• Solve the last two kinds of dependencies by using a modified Tomasulo algorithm
Critique

• Pros
  – Out-of-order execution capability
  – A modified Tomasulo algorithm is proposed

• Cons
  – Figures are very unclear
  – No experimental results
Question

• What is the performance?
• Is it still practical now or in the future?
• How to deal with the high bandwidth requirement?