21264

- 7 pipeline stages
  - At the time: PII-300mhz, Alpha 500-Mhz
- Width = 4
  - Fetch 4/cycle
  - Issue 4+2/cycle
    - 4 integer or load/stores
    - 2 floating point
  - Completion
    - At most 11, 8 over awhile
- Branch predictor
  - Predictor selection
  - Speculative history
- Physical register file: 80 integer (doubled for the cluster)

P4

- 20 pipeline stages +/- a few
  - 20 after the trace cache
  - Several
- Everything ever invented
  - Trace cache
  - OOO
  - “Highly advanced” branch predictor
  - 100mhz, 400mhz, 750Mhz, 1.5Ghz, 3Ghz
- Completion: 3/cycle uops
- Issue: 6/cycle uops

P5

- 64 bit
- “Designed by the AMD subsidiary of Intel”
- An even more advanced hyper netbursting-branch predictor
- Crazier streaming media applications
- Secure net transactions?
- Maybe virtualizable
- New bug
- A CMP of SMT’s (Microcluster of Hyperthreaded Processors)