Cyber 180-990

• New high performance processor
  – Deep pipeline
  – Code compatibility with this whacky 60 bit machine
  – Vector memory->memory instructions
• Fetch 6 stages, 5 minimum in execution
Branch prediction: what and why

• Why: otherwise we stall or have useless delay slots

• What: Making a guess on a branch outcome in the fetch stage of a processor
What do you do on a mispredict?

• Undo
• Change program to correct value
• Flush away invalid instructions
• Return machine state to as if had not been executed
  – Prevented speculative instructions from completing.
What else can we do besides predict?

- $2^n$ brute force execution
- Unrolling
  - Less prediction/Time
  - Not smart unrolling pollutes table
- LOOPZ