How to speak pigeon

- FLR = register
- CDB = common data bus
- *sink* = destination register
- FLB/SDB = reservation stations
- FLOS = processor
What was wrong with score-boarding?

- Instruction can stall
- Waiting too long for operands
- Centralized hazard detection and resolution
- Stall for WAW and WAR hazards
When can we execute an instruction?

- When you have operands and an execution core
Cardinal Precedence Principle

• No floating point register may participate in an operation if it is the sink of another incomplete instruction
• Values must available
3 Things hardware must support..

• (1) Detect data dependencies
• (2) Dataflow has to be preserved
• (3) When you can execute out-of-order you should
What is a “reservation station”?

• Control
  – Operation
  – Source register #'s
  – Valid bit
  – Target register #

• Data
  – Actual data items

• Other
  – Count value for scheduling
Mem -> Issue Window

• **WaitFor**
  – Space in the queue
  – Have the instruction from the memory

• **Do**
  – Decoding (if you want)
  – Place in queue
Issue Window -> Issue

- **WaitFor**
  - Need a free reservation station

- **Do**
  - Put instruction there
  - Transform them from architectural registers to tags, or, read value from register file
  - Set register file valid bit to zero and put tag of reservation station in register file.
Issue -> Execute

• WaitFor
  – Have all your data valid (all tags broadcasted)
  – A free execution uni

• Do
  – Execute!
Execute -> complete

- **WaitFor**
  - Waiting for a result bus to be free
  - Execute to complete

- **Do**
  - Send value and tag on result bus
Advantages

• More concurrent execution and still have order of precedence
  – Avoids WAR, WAW, and RAW hazards
• Research: use as a scheduler for a compiler
• Less reliance on those lousy compilers
Disadvantages

• Does not exploit associativity
  – $A = b[0] + b[1]$  
  – $A = A + b[2]$  
  – $A = A + b[3]$  

• Complex: Full employment act for architects
O(n) structures/functions

- E functional units
- R reservation stations
- I issues per cycle
- W word size of the machine
- C CDB busses
- A architectural registers
structures/functions

• Renaming $O(I \times (2 \times \log(A) + \log(R) + \log(A)) + I^2 \times \log(A))$

• Reservation station to execute $O(R \times E \times 3W)$

• Execute -> Complete
  – $O(E \times C \times (W + \log(R)))$
Space Complexities

• Tomasulo
  - Check of RAT
  - Check of Reservation-Queue is
  - Send result to completion bus
  - Completion bus(s) to reservation station
  - Complexity of Load/Store buffer

• Multiple-In-Order-Issue Tomasulo
  - Check of RAT
Load/Store

- Total Load-Store ordering
- Relaxed memory model architectures
- Do more per cycle
- Check queue and satisfy early (possibly)
- Speculate
- Punt its up to the programmer