Computer Design & Organization
Assignment 1
Due: Wednesday, October 6

The purpose of this assignment is to acquaint you with the sim-outorder simulator that is part of the SimpleScalar tool set and the environment in which it executes. Sim-outorder is an instruction-level simulator that implements many of the architectural features we will study this quarter. But for this assignment, we will use it as though it looks very much like the R3000 you studied in CSE378. Sim-outorder implements the SimpleScalar instruction set architecture, which is very similar to the MIPS architecture.

For this assignment you are expected to work in teams of 2 people. By the way most assignments will involve 2-person teams. For each assignment you should work with a different set of partners, so begin planning ahead for your partners. If there is an odd number of students in the class, the solo should change for each assignment. Please turn in one report per pair and remember to put both partner names on the report. If you decided to divide up the work, say who did what.

For this assignment, you should:

1. Pick an application from the application directory to instrument. All these programs are taken from the SPEC95 benchmark suite, which was the standard workload for architecture research two suite-generations ago (we are now on SPEC2000). They have already been precompiled for sim-outorder and you can use them as input to the simulator. Douglas will send you email if it turns out that any of the applications are not appropriate for this assignment.
2. Set sim-outorder configuration parameters to reflect a computer that has the following configuration:
    - a pipeline that fetches, decodes, issues, executes and commits one instruction/cycle, no matter what the instruction type
    - only one of each type of functional unit
    - an 8KB, two-way set-associative L1 instruction and data caches with 32 byte blocks
    - a 256KB, direct-mapped L2 unified cache with 32 byte blocks
    - an 8-way, 128-entry data TLB
    - a 4-way, 64-entry instruction TLB
    - All caches and the TLB have an LRU block replacement policy.
    - The page size is 4KB.

    This means that the rest of the parameters should be left with their default values, except for two which must be set to: fetch:speed 1 and issue:inorder true. The configurations are set by command line arguments or sim-outorder's config file.

Answer or do the following:

1. Report the configuration parameters you used, which will be either a configuration file or command line parameters. (1 point)
2. Highlight and label the values for the following metrics on your sim-outorder output: (3 points)
    - total number of instructions committed – this is all the instructions that have completed all the phases of instruction execution, including writing their results to the register file.
    - the total number of block replacements for the L1 data cache
    - the hit ratio for the L2 cache
3. Answer the following questions: (3 points each)
    - What is the rationale for the value for the number of cycles per instruction?
    - Why is there a difference between the number of blocks replaced in the L1 data cache and the number of blocks written back from the L1 data cache?
    - Justify the value of the total number of write-backs for the L1 instruction cache.

There is no electronic turn-in required for this assignment. Instead bring to class on October 6 paper copies of the output generated by sim-outorder and your answers to the questions.