CSE 471 Autumn 2001

Computer Design and Organization

Tentative Outline

This document will be evolving during the course of the quarter. We won't have the time to look at everything! Also, I might add some new references from time to time.

1. Review of pipelining, cache organization, and common metrics for the performance of computer systems
   References:
   - Hennessy and Patterson: *Computer Organization and Design*, aka the CSE378 book; In particular, see Chapters 6 and 7.
   - In this quarter's textbook see Chapter 3 Sections 1 through 5, Chapter 5 Sections 1 and 2, and Chapter 1 Section 5.
   - J.Smith "Characterizing Computer Performance with a Single Number" CACM vol 31, 10, Oct 1988 pp 1202-1206
   - For information on Spec benchmarks see http://www.specbench/org/
2. Branch prediction. Static schemes. Dynamic branch prediction and branch-prediction buffers. Two-level branch prediction. Branch target buffers.
   References:
   - In this quarter's textbook see Chapter 4 Section 3
   - D. Lilja "Reducing the Branch Penalty in Pipelined Processors" IEEE Computer, July 1988, pp 47-55
   - T-S. Yeh and Y.Patt "A Comparison of Dynamic Branch Prediction that use Two Levels of Branch History" Proc. 20th Int. Symp. Computer Architecture, 1993, pp 257-266
3. Exceptions in simple pipelines
   References:
   - In this quarter's textbook see Chapter 3 Section 6
4. Single issue machine with multiple pipes
   References:
   - In this quarter's textbook see Chapter 3 Section 7

5. Instruction level parallelism - Introduction.
   References:
   - In this quarter's textbook see Chapter 4 Section 1
6. Dynamic scheduling.
   - Scoreboard
   - Tomasulo's algorithm. Register renaming. Out of order execution and in-order completion.

   References:
   - In this quarter's textbook see Chapter 4 Section 2
7. Superscalar processors. Multiple instruction issue. The instruction fetch unit.
   References:
   - In this quarter's textbook see Chapter 4 Section 4
   - **a MUST read** J.Smith and G. Sohi "The Architecture of Superscalar Microprocessors" Proc. IEEE, 83,12, Dec 1995.
8. VLIW and EPIC
   References:
   - M.Schlansker and B. Rau "EPIC: Explicitly Parallel Instruction Computing", Computer, Feb 2000, 37-45
   - A presentation of the Intel Itanium can be found at:

     `http://developer.intel.com/design/ia64/microarch_ovw/sld001.htm`
9. Multithreading. Coarse grain vs. fine grain. Simultaneous Multithreading (SMT).
   References:
   - G.Alverson, R.Alverson, D.Callahan, B.Koblenz, A.Porterfield, and B.Smith "Exploiting Heterogeneous Parallelism on a Multithreaded Processor" Proc. ICS, 1992, pp 188-197
   - D.Tullsen, S.Eggers, and H.Levy "Simultaneous Multithreading: Maximizing On-Chip Parallelism", Proc. ISCA 1995, pp 392-403
10. Cache hierarchies.
    References:
    - In this quarter's textbook see Chapter 4 Sections 1 through 5
11. Cache optimizations (write buffers, lock-up free caches, victim caches, prefetching etc.)
    References:

- For historical details about caches and a private anthology, you can look at slides 1-20 of a talk I gave two years ago at HPCA.

  `http://www.cs.washington.edu/homes/baer/hpca6.ppt`

12. Main memory (interleaving, page mode, synchronous memory, Rambus).
    References:

    - In this quarter's textbook see Chapter 5 Section 6
    - R.Crisp "Direct Rambus technology: The New Main Memory Standard" IEEE Micro, Nov 1997, pp 18-28.

13. Virtual memory and TLB management
    References:

    - In this quarter's textbook see Chapter 5 Sections 7 through 10
    - B.Jacob and T.Mudge "Virtual Memory in Contemporary Microprocessors" IEEE Micro, July 1998, pp 60-75

14. Buses. Arbitration. Split-transaction.
    References:

    - In this quarter's textbook see Chapter 6 Section 3

15. Disks. RAIDs.
    References:

    - In this quarter's textbook see Chapter 6 Section 5
    - C.Ruemmler and J.Wilkes "An Introduction to disk Drive Modeling", IEEE Computer, March 1994, 17-28

16. Shared-memory multiprocessors. Teminology (Shared-bus, SMP, NUMA).
    References:

    - In this quarter's textbook see Chapter 8 Section 1

17. Cache coherence in SMP's
    References:

    - In this quarter's textbook see Chapter 8 Section 3