Computer Design and Organization

Tentative Outline

This document will be evolving during the course of the quarter. We won’t have the time to look at everything! Also, I might add some new references from time to time.

1. Review of pipelining, cache organization, and common metrics for the performance of computer systems
   References:
   - Hennessy and Patterson. Computer Organization and Design, aka the CSE378 book; In particular, see Chapters 6 and 7.
   - In this quarter’s textbook see Chapter 3 Sections 1 through 5, Chapter 5 Sections 1 and 2, and Chapter 1 Section 5.
   - For information on Spec benchmarks see http://www.specbench.org/

2. Branch prediction. Static schemes. Dynamic branch prediction and branch-prediction buffers. Two-level branch prediction. Branch target buffers. References:
   - In this quarter’s textbook see Chapter 4 Section 3
   - D. Lilja “Reducing the Branch Penalty in Pipelined Processors” IEEE Computer, July 1988, pp 47-55

3. Exceptions in simple pipelines
   References:
   - In this quarter’s textbook see Chapter 3 Section 6

4. Single issue machine with multiple pipes
   References:
   - In this quarter’s textbook see Chapter 3 Section 7
5. Instruction level parallelism - Introduction.
   References:
   • In this quarter's textbook see Chapter 4 Section 1

   • Scoreboard
   • Tomasulo's algorithm. Register renaming. Out of order execution and in-order completion.
   References:
   • In this quarter's textbook see Chapter 4 Section 2

7. Superscalar processors. Multiple instruction issue. The instruction fetch unit.
   References:
   • In this quarter's textbook see Chapter 4 Section 4

8. VLIW and EPIC
   References:
   • A presentation of the Intel Itanium can be found at:
     http://developer.intel.com/design/ia64/microarch_ovw/sld001.htm

   References:

    References:
    • In this quarter's textbook see Chapter 4 Sections 1 through 5

11. Cache optimizations (write buffers, lock-up free caches, victim caches, prefetching etc.)
    References:
• For historical details about caches and a private anthology, you can look at slides 1-20 of a talk I gave two years ago at HPCA.

   References:
   • In this quarter’s textbook see Chapter 5 Section 6

13. Virtual memory and TLB management
   References:
   • In this quarter’s textbook see Chapter 5 Sections 7 through 10
   • B. Jacob and T. Mudge “Virtual Memory in Contemporary Microprocessors” IEEE Micro, July 1998, pp 60-75

   References:
   • In this quarter’s textbook see Chapter 6 Section 3

15. Disks. RAID.
   References:
   • In this quarter’s textbook see Chapter 6 Section 5

   References:
   • In this quarter’s textbook see Chapter 8 Section 1

17. Cache coherence in SMP’s
   References:
   • In this quarter’s textbook see Chapter 8 Section 3