Nehalem

Intel Micro-architecture

Features:

- Wide Dynamic Execution:

  Every processor core can fetch, dispatch, execute and retire up to four instructions per clock cycle.

- Advanced Smart Cache:

  improved bandwidth from the second level cache to the core, and improved support for single- and multi-threaded applications computation.

- Smart Memory Access:

  which pre-fetches data from memory responding to data access patterns, reducing cache-miss exposure of out-of-order execution.

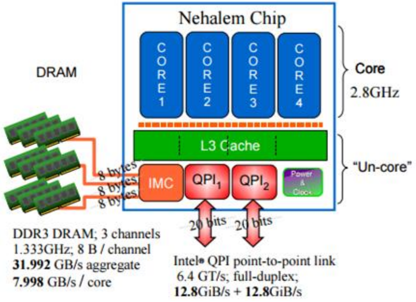
- Advanced Digital Media Boost:

  for improved execution efficiency of most 128-bit SIMD instruction with single-cycle throughput and floating-point operations.

Instruction and Data Flow Process:

- The early stages of the processor **fetch**-in several macro-instructions at a time.
- **decode** them into sequences of micro-ops.
- The micro-ops are buffered at various places where they can be picked up and scheduled to use in parallel if data dependencies are not violated. In Nehalem, micro-ops are issued to stations where they reserve their position for subsequent.
- dispatching as soon as their input operands become available.
- Finally, completed micro-ops retire and post their results to permanent storage.

Hardware impelementation



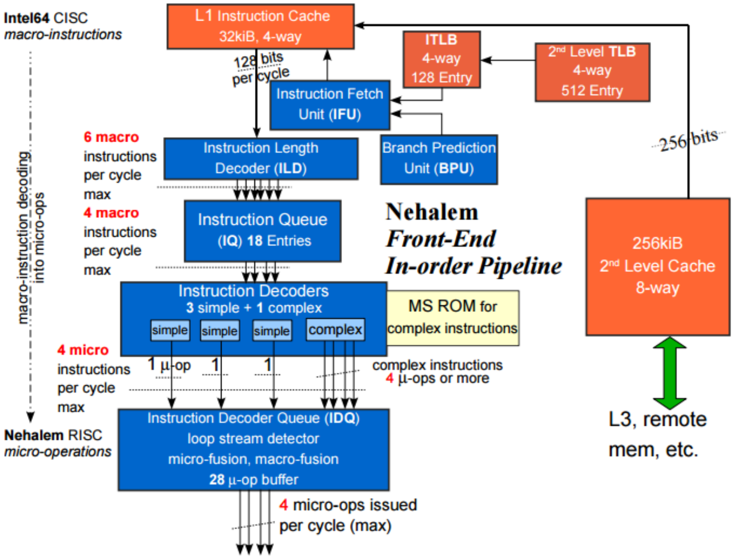
- four identical compute cores
- UIU: Un-Core Interface Unit (switch connecting the 4 cores to the 4 L3 cache segments, the IMC and QPI ports)
- L3: level-3 cache controller and data block memory
- IMC: 1 integrated memory controller with 3 DDR3 memory channels
- QPI: 2 Quick-Path Interconnect ports
- auxiliary circuitry for cache-coherence, power control, system management and performance monitoring logic

Software Access

- a 64-bit linear (“flat”) logical address space,
- uniform byte-register addressing,
- 16 64-bit-wide General Purpose Registers (GPRs) and instruction pointers
- 16 128-bit “XMM” registers for streaming SIMD extension instructions, in addition to 8 64-bit MMX registers or the 8 80-bit x87 registers, supporting floating-point or integer operations,
- fast interrupt-prioritization mechanism,
- a new instruction-pointer relative-addressing mode.

Front-End In-order Pipeline

- Retrieve blocks of macro-instruction from memory
- Translate instruction
- Handle instruction in-order
- Decode 4 instruction per cycle
- Decode instruction streams of threads in alternate cycles


Intel64 CISC
macro-instructions
L1 Instruction Cache
32kiB, 4-way
128 bits per cycle
ITLB
4-way
128 Entry
2nd Level TLB
4-way
512 Entry
Instruction Fetch Unit (IFU)
256 bits
6 macro instructions per cycle max
Instruction Length Decoder (ILD)
Branch Prediction Unit (BPU)
4 macro instructions per cycle max
Instruction Queue (IQ) 18 Entries
Nehalem Front-End In-order Pipeline
256kiB
2nd Level Cache
8-way
macro-instruction decoding into micro-ops
Instruction Decoders
3 simple + 1 complex
simple
simple
simple
complex
MS ROM for complex instructions
4 micro instructions per cycle max
1 µ-op
1
1
complex instructions
4 µ-ops or more
L3, remote mem, etc.
Nehalem RISC
micro-operations
Instruction Decoder Queue (IDQ)
loop stream detector
micro-fusion, macro-fusion
28 µ-op buffer
4 micro-ops issued per cycle (max)

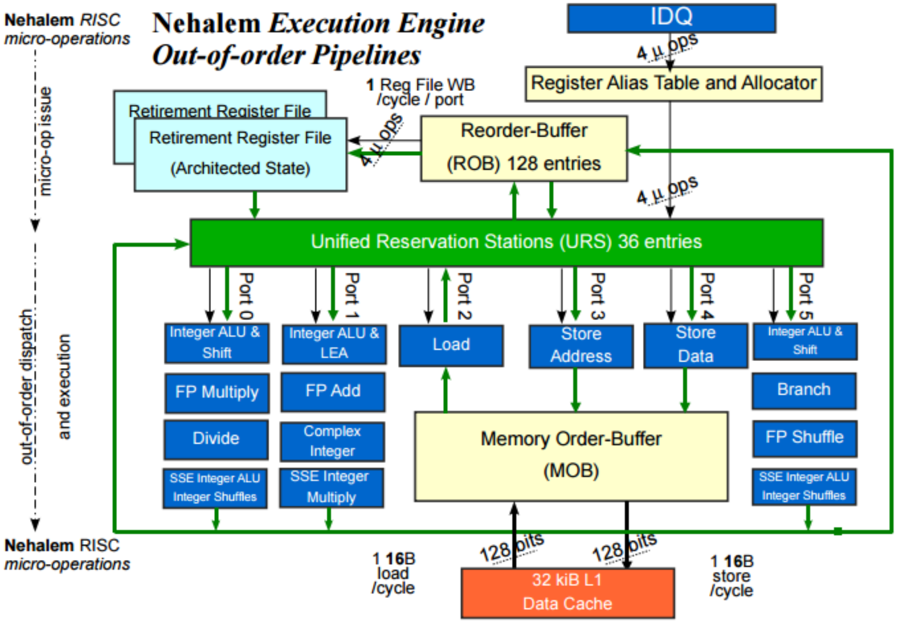
Execution Engine Out-of-order Pipelines

- -Dynamically schedule micro-ops for dispatching and excution

- Dispatch up to 6 micro-ops per cycle

- Foure micro-ops can retire per cycle

- Result written-back rate up to one register per port per cycle


Nehalem RISC micro-operations
Nehalem Execution Engine Out-of-order Pipelines
IDQ
4 µ ops
Register Alias Table and Allocator
1 Reg File WB /cycle / port
Retirement Register File
Retirement Register File (Architected State)
4 µ ops
Reorder-Buffer (ROB) 128 entries
4 µ ops
micro-op issue
Unified Reservation Stations (URS) 36 entries
Port 0
Port 1
Port 2
Port 3
Port 4
Port 5
Integer ALU & Shift
Integer ALU & LEA
Load
Store Address
Store Data
Integer ALU & Shift
FP Multiply
FP Add
Branch
Divide
Complex Integer
Memory Order-Buffer (MOB)
FP Shuffle
SSE Integer ALU Integer Shuffles
SSE Integer Multiply
SSE Integer ALU Integer Shuffles
out-of-order dispatch and execution
Nehalem RISC micro-operations
1 16B load /cycle
128 bits
128 bits
1 16B store /cycle
32 kiB L1 Data Cache