IBM System/360

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Overview

Series of Large Mainframe Computers

Series Compatible

Upgradeable

Openly Available to purchase
“Solid Logic Technology”
Trends

Established 8 bits as a byte

Byte Addressable Memory (opposed to bit addressable)

Aftermarket peripherals

The upgradeable computer and backwards compatibility
Efficient Algorithm for Multiple Arithmetic Units

Floating point operations very slow

Planned for Multiply 6 cycles, Divide 18 cycles, Add 2 cycles

Abstract data path into pseudo-register-to-register format

Goal: Parallel execution of independent operations

1. Recognize the existence of dependencies
2. Correctly sequence dependent instructions
3. Must distinguish between dependent sequences and independent sequences

Preservation of precedence: busy bit

Illusion of Multiple Redundant Units: reservation station