IBM 360

& Tomasulo’s Algorithm
Amdahl’s parallelism law: If a computation has a serial component S and a parallel component P, then the maximum speedup is (S+P)/S.

Amdahl’s balanced system law: A system needs a bit of IO per second for each instruction per second: about 8 MIPS per MBps.

Amdahl’s memory law: In a balanced system the MB/MIPS ratio is 1.

Amdahl’s IO law: Programs do one IO per 50,000 instructions.
Innovations?

• Out of order execution (Tomasulo's Algorithm)
• Page-based virtual addressing (memory)
• Availability of a family of I/O devices
• Architecture as we know it
  • separation of microarchitecture and architecture
  • or implementation and ISA
• Operating system
• Shared storage device
• The byte.
Robert Tomasulo
Tomasulo’s Algorithm

- Uncovered instruction level parallelism

- for (i = 0; ; i++) a[i] = a[i] + r2;

- HERE:
  LOAD @(r4) - > R1
  ADD R1, R2 -> R1
  STORE R1 -> @(r4)
  ADD #1, R4 -> R4
  JUMP HERE

- LOAD @(r4) - > R1
  ADD R1, R2 -> R1
  STORE R1 -> @(r4)
  ADD #1, R4 -> R4
  LOAD @(r4) - > R1
  ADD R1, R2 -> R1
  STORE R1 -> @(r4)
  ADD #1, R4 -> R4
  JUMP HERE
LOAD @r4 -> R1
ADD R1, R2 -> R1
STORE R1 -> @r4
ADD #1, R4 -> R4
LOAD @r4 -> R1
ADD R1, R2 -> R1
STORE R1 -> @r4
ADD #1, R4 -> R4
JUMP HERE

LOAD @(r4), P5
ADD P5, P2, P6
STORE P6, @(P4)
ADD #1, P4, P7
LOAD @(P7), P8
JUMP HERE

MAP: R1:P1, R2:P2, R3:P3, R4:P4
FREE-LIST: P5, P6, P7, P8, ....
Figure 1 Data registers and transfer paths without CDB.
Figure 4 Data registers and transfer paths, including CDB and reservation stations.
Troubles with Out of Order Execution ala Tomasulo’s Alg.

• Big

• Out of execution leads to exception problems

• Matching software to hardware resources
Fred Brooks