**Collaboration Policy:**

The final project represents your individual effort to design a chip. You may discuss your project with other CSE 468/568 students, but the design, analysis, layout, and turn-in must be entirely your own work. You may not use partial results from other students’ projects (such as simulation results or cell layouts) in your project.

**Late Project Policy:**

We cannot accept late projects. If you do not present your project to the instructor and turn in a written report by March 15, you will either receive an incomplete or not pass the class, depending on the circumstances.

**What You Must Do:**

Design, analyze, simulate, layout, back-annotate, DRC, and LVS a sequential (clocked or self-timed) integrated circuit comprising at least 1000 transistors, using the TSMC 0.35\( \mu \)m CMOS process. **You must layout your project in an 84-pin padframe that you create. Your entire design must pass LVS (at the padframe level).** Your project may be any reasonable digital circuit of your own choosing (if you have questions about the word "reasonable", consult with the instructor). We will work with you to ensure appropriate project selection.

**Grading:**

We will grade your project based on the overall design (circuit details, including project difficulty and circuit cleverness), your simulation results (speed and proper use of tools), your layout (layout practices, device sizing, power/gnd sizing, etc.), and the completeness and clarity of your written report. **Your design must pass DRC and LVS at the padframe level. You must also complete a back-annotated simulation (with parasitics) of your design.** We will supply you with mini-deadlines along the way to help you stay on track. These deadlines will have some grade (points) associated with them, so it is in your best interest to stay up to speed.

**What You Must Turn In:**

You must hand in a complete written description of your project including motivation, schematics (human readable), key statistics (area, power consumption, etc), design insights, simulation results, proof of DRC/LVS completion, and any other information you deem necessary.

You will hand in your report during a final project interview (to be scheduled with the instructors during finals week) during which you will demo your project and take questions from the instructors.