DDR3 Synchronous DRAM Memory

- DDR data transfer
- Burst read and write
- Simultaneous multiple bank operation
- Command sequencing and pipelining
- Read/Write leveling
Figure 4: 256 Meg x 8 Functional Block Diagram
8-bit prefetch/burst length

Since 8 bits at a time are read from DDR3 memory into the I/O buffer, so even if the data bus is handling transfer at a rate of 1066 Mbps, the internal bus operating at 133 MHz will be capable of handling this if there is little other load, so high-speed operation is realized.

With the external clock 4 times of internal clock, transfer 8 bits every half-clock cycle.

Transfer 8 bits per clock cycle.

DDR3 Synchronous DRAM
Commands

✦ PRECHARGE
  ✦ Ready BANK for an ACTIVATE (closes currently active row)
  ✦ Read and Write may issue an auto-precharge

✦ ACTIVATE
  ✦ Open a ROW in a BANK for access (Row Address)
  ✦ ROW remains active until a Precharge

✦ READ
  ✦ Initiate a burst read from an active ROW in a BANK

✦ WRITE
  ✦ Initiate a burst write to an active ROW in a BANK

✦ REFRESH/SELF REFRESH
Figure 2: Simplified State Diagram

ACT = ACTIVATE
MPR = Multipurpose register
MRS = Mode register set
PDE = Power-down entry
PDX = Power-down exit
PRE = PRECHARGE
PREA = PRECHARGE ALL
SEX = Self refresh exit
WRITE = WR, WR5, WR6
WRITE AP = WRAP, WRAP5, WRAP6
ZQCL = ZQ LONG CALIBRATION
ZQCS = ZQ SHORT CALIBRATION

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Reads

Figure 67: READ Latency

Figure 68: Consecutive READ Bursts (BL8)
Writes

Figure 85: Consecutive WRITE (BL8) to WRITE (BL8)
### Commands – Truth Tables

**Table 69: Truth Table – Command**

Notes 1–5 apply to the entire table.

<table>
<thead>
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<td>L</td>
<td>BA</td>
<td>RFU</td>
<td>V</td>
<td>L</td>
<td>CA</td>
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<td>H</td>
<td>L</td>
<td>BA</td>
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<td>L</td>
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<td>ZQ CALIBRATION LONG</td>
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<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
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<td>ZQCS</td>
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<td>X</td>
<td>L</td>
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Mode Registers

- Burst length: 4/8/dynamic
- READ burst type: Sequential/Interleaved

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<th>Mode</th>
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<td>0 1 1</td>
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<tr>
<td>1 1 0</td>
<td>1 1 1</td>
<td>1 1 1</td>
</tr>
<tr>
<td>1 1 1</td>
<td>WRITE</td>
<td>WRITE</td>
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<tr>
<th>Mode</th>
<th>Burst Length</th>
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</thead>
<tbody>
<tr>
<td>WRITE</td>
<td>0 1 2 3 4 5 6 7</td>
</tr>
</tbody>
</table>

- Write Recovery: clock cycles
Mode Registers (cont)

✦ CAS Read Latency: clock cycles READ to data output

Figure 53: READ Latency
Mode Registers (cont)

- Additive Latency
  - Allows ACTIVATE – READ/WRITE to be done together
  - AL holds back READ/WRITE for n clock cycles
Mode Registers (cont)

✦ CAS Write Latency

Figure 57: CAS Write Latency

BC4

Indicates A Break in Time Scale  Transitioning Data  Don’t Care

DDR3 Synchronous DRAM
“Fly-by” clocking – Source Synchronous

DDR3 Synchronous DRAM
“Fly-by” and Read Leveling

DDR3 Synchronous DRAM

**MPR (DRAM)**
Output known pattern (set by MR)

(Exp.)
- Burst length: 8
- Burst order: 0, 1, 2, 3, 4, 5, 6, 7
- Pre-defined pattern: [0, 1, 0, 1, 0, 1, 0, 1]

**Read leveling (Controller)**
Estimate skew (delay) of DQ, DQS, and DM

DDR3 Synchronous DRAM
Write-Leveling

Figure 1-7 Conceptual Diagram of Write Leveling
Memory Bandwidth

- Accesses to same row are fast
  - Back-to-back reads/writes to row

- Changing rows costs time
  - PRECHARGE/ACTIVATE

- Multiple bank accesses can be overlapped
  - Interleave bank accesses
  - Pipeline/overlap PRECHARGE/ACTIVATE
  - Good for random access