Source Synchronous

Clock skew may be significant
\( S_0 \) may be large
\( \Rightarrow \) Very slow clock.

Idea: Match delays; Send clock with data!

Note: \( S_0 \) can be larger than clock period!

We still have a problem...
We now have arbitrary skew between the source clock and system clock. Solution?

1. Acquire the async. FIFO (problem?)
2. Compute phase difference fixed?