Clocking Magic with PLLs
Phase-Locked Loop

VCO - Voltage Controlled Oscillator
  - e.g. Ring oscillator
  - Higher V_{in} → Faster operation
  - e.g. Freq = 1.6 GHz → 3.2 GHz

Phase Comparator: Depending on phase difference, increase/decrease voltage

Reference

Feedback

Too fast → decrease V
Too slow → increase V

Use #1: Generate Multiple Frequencies

\[ \frac{f_{REF}}{A} \sim \frac{f_{VCO}}{B} \]

\[ f_{VCO} = f_{REF} \times \frac{B}{A} \]

By programming A & B, we can choose \( f_{VCO} \) almost arbitrarily.
Use #2: Generate Multiple Related Frequencies

- VCO
- GEN1
- GEN2

Clock Generators
Programmable Waveforms
Programmable Phases

Use #3: Clock Insertion Delay Compensation

Chip clock tree: Balance delay

Clock arrives at all registers about the same time.

Some skew is inevitable.

However, there is a large insertion delay.

Solution: Ref

Hatched delay clock tree

PLL "copies" Reference clock to Local clock.