Synchronous FIFO

Data In -> MEM tail -> head -> Data Out

dVIn

tIn

clkIn

Clock Domain Crossing

How do you tell this isn't an
asynchronous FIFO?

What are the problems?
* Head tail cross clock domains
  + Add "synchronizers"
* Can't synchronize multiple bits
  + Use Gray Code

Note: \( (\text{head} \neq \text{tail} \cdot 1) \equiv (\text{head} \cdot 1 \neq \text{tail}) \)