The Primary Problem with Asynchronous Inputs

- What goes wrong here? (Hint: it’s not a metastability thing)
Another Problem with Asynchronous inputs

- What goes wrong here? (Hint: it’s not a metastability thing)
  - Slight delay differences mean that the registers can disagree on the input value
  - “Inconsistent value problem”
More Asynchronous Inputs

- What is the problem?
- “Inconsistent value problem”
  - Two paths from input to two different registers
**Important Rule!**

- Exactly one register makes the sampling decision
  - Where it enters the clock domain
  - Completely solves the “inconsistent value problem”
Sampling external inputs

CLKA
Q(A)
CLKB
Q(B)

0 0 0/1? 1 1

clkA
clkB
Doesn’t matter which the register decides
There is a clean 0 → 1 on the input
Problem: Register sometimes can’t decide
The Metastability problem
"Synchronizer"

- We sample with a register pair
- Maximizing the resolution time
What does this circuit trying to do?

- What’s wrong with it?
Two registers before we use the signal

- How much better is this?
Stretching the Resolution Time

- Also slows the sample rate / transfer rate
**Sampling Rate**

- How fast does your sample clock need to be?
**Sampling Rate**

- How fast does your sample clock need to be?
  - $f(\text{clkB}) > f(\text{clkA})$
  - $f(\text{clkB}) > 2 f(\text{data})$ (Nyquist)
More Asynchronous Inputs

- Can we input asynchronous data values with several bits?
More Asynchronous inputs

- How can we input asynchronous data values with several bits?

```
CLKA
Q(A)[7:0]  x00  xFF
CLKB
Q(B)[7:0]  x00  x00  x00/xFF  xFF  xFF
Q(C)[7:0]  x00  x00  x00  xAA  xFF
!!
```
What Went Wrong?

- Each bit has a different delay
  - Wire lengths differ
  - Gate thresholds differ
  - Driver speeds are different
  - Register delays are different
    - Rise vs. Fall times
    - Clock skews to register bits
- Bottom line – “data skew” is inevitable
  - aka Bus Skew
  - Longer wires => More skew
- What is the solution??
**Sending Multiple Data Bits**

- Must send a “clock” with the data
  - Waits until data is stable
  - De-skewing delay
- \( f(\text{clkB}) > 2 f(\text{clkA}) \)
Sending Multiple Data Bits

- Balancing path delays can increase data rate
- Requires careful analysis of clock rates and delays to make sure data is stable when sampled
**Sending Multiple Data Bits**

- Slightly different alternative . . .