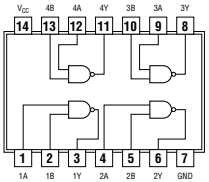
Pin Assignments

00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

positive logic:

$Y = \overline{A \cdot B}$

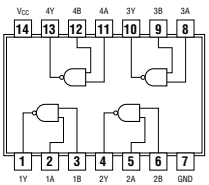


See page 139

01
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$Y = \overline{A \cdot B}$

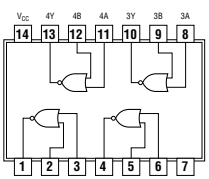


See page 140

02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

positive logic:

$Y = \overline{A + B}$

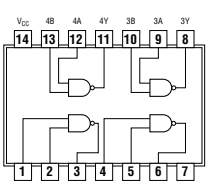


See page 141

03
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$Y = \overline{A \cdot B}$

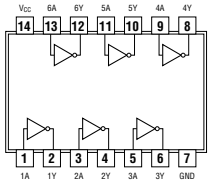


See page 142

04
HEX INVERTERS

positive logic:

$Y = \overline{A}$

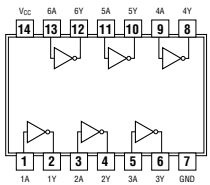


See page 143

U04
HEX INVERTERS

positive logic:

$Y = \overline{A}$

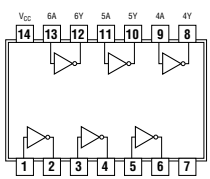


See page 144

05
HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$Y = \overline{A}$

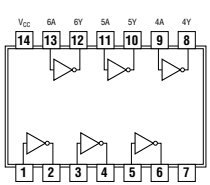


See page 144

06
HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

positive logic:

$Y = \overline{A}$



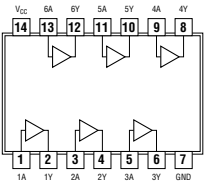
See page 145

07

HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

positive logic:

$Y = \overline{A}$



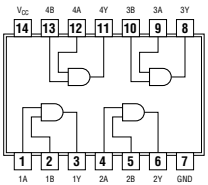
See page 145

08

QUADRUPLE 2-INPUT POSITIVE-AND GATES

positive logic:

$Y = A \cdot B$



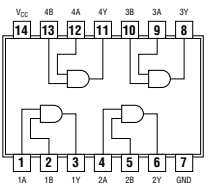
See page 146

09

QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$Y = A \cdot B$



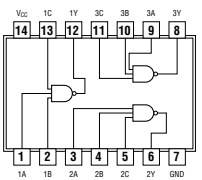
See page 147

10

TRIPLE 3-INPUT POSITIVE-NAND GATES

positive logic:

$Y = \overline{A \cdot B \cdot C}$



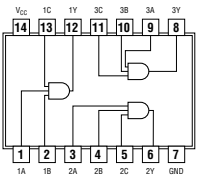
See page 148

11

TRIPLE 3-INPUT POSITIVE-AND GATES

positive logic:

$Y = A \cdot B \cdot C$



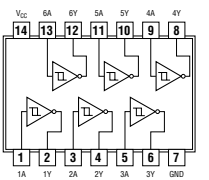
See page 149

14

HEX SCHMITT-TRIGGER INVERTERS

positive logic:

$Y = \overline{A}$



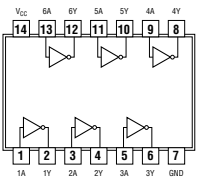
See page 150

16

HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

positive logic:

$Y = \overline{A}$



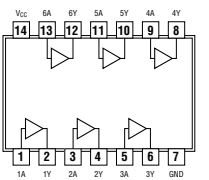
See page 151

17

HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

positive logic:

$Y = A$



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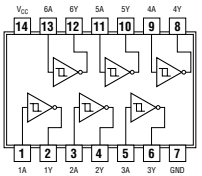
Pin Assignments

19

HEX SCHMITT-TRIGGER INVERTERS

positive logic:

$Y = \overline{A}$



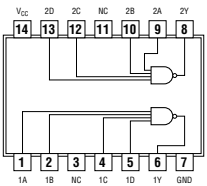
See page 152

20

DUAL 4-INPUT POSITIVE-NAND GATES

positive logic:

$Y = \overline{A \cdot B \cdot C \cdot D}$



NC – No internal connection

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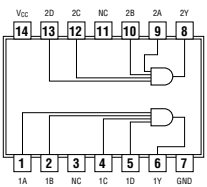
21

DUAL 4-INPUT POSITIVE-AND GATES

positive logic:

$Y = A \cdot B \cdot C \cdot D$



NC – No internal connection

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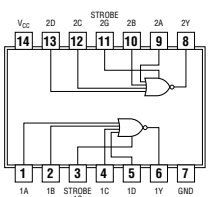
25

DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

positive logic:

$Y = G\,(\overline{A + B + C + D})$



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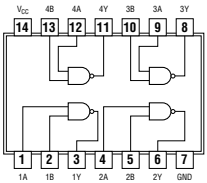
26

QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

positive logic:

$Y = \overline{AB}$



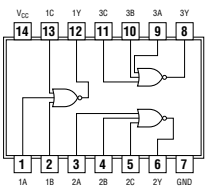
See page 155

27

TRIPLE 3-INPUT POSITIVE-NOR GATES

positive logic:

$Y = \overline{A + B + C}$



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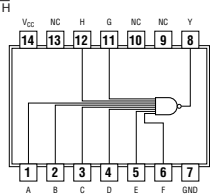
30

8-INPUT POSITIVE-NAND GATES

positive logic:

$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$



NC – No internal connection

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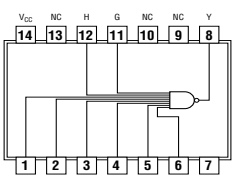
31

DELAY ELEMENTS



NC – No internal connection

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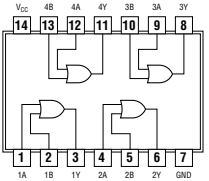
32

QUADRUPLE 2-INPUT POSITIVE OR GATES

positive logic:

$Y = A + B$



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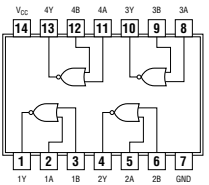
33

QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$Y = \overline{A + B}$



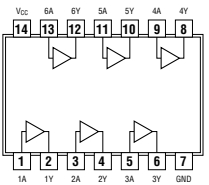
See page 158

35

HEX NONINVERTERS WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$Y = A$



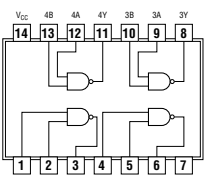
See page 158

37

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

positive logic:

$Y = \overline{A \cdot B}$



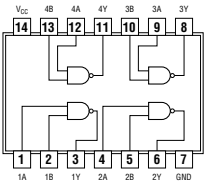
See page 159

38

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

positive logic:

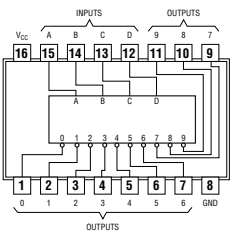
$Y = \overline{A \cdot B}$



See page 159

42

4-LINE-TO-10-LINE DECODERS



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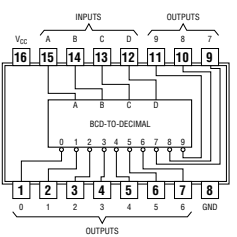
45

BCD-TO-DECIMAL DECODER/DRIVER



See page 162

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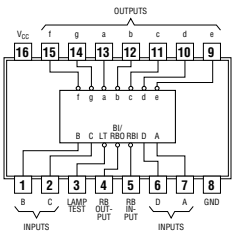
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS



See page 164

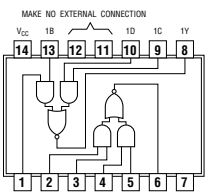
51

AND-OR-INVERT GATES

'51, 'S51 DUAL 2-WIDE 2-INPUT

positive logic:

$Y = \overline{AB + CD}$



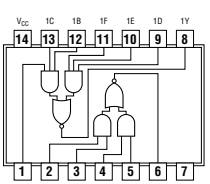
AND-OR-INVERT GATES

'LS51 2-WIDE 3-INPUT, 2-WIDE 2-INPUT

positive logic:

$1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$

$2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$



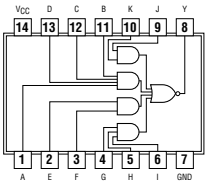
See page 166

64

4-2-3-2 INPUT AND-OR INVERT GATE

positive logic:

$Y = \overline{ABCD + EF + GHI + JK}$



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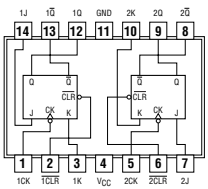
DUAL J-K FLIP-FLOPS WITH CLEAR



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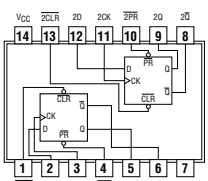
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR



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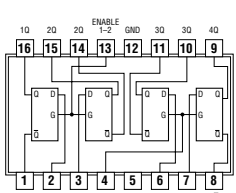
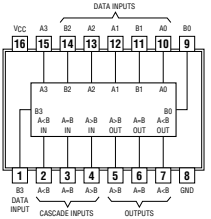
4-BIT BISTABLE LATCHES



See page 172

85
4-BIT MAGNITUDE COMPARATORS

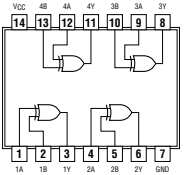


See page 173

86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

positive logic:

$Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$



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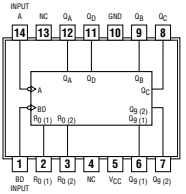
90
DECADE COUNTER



NC – No internal connection

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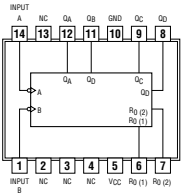
92
DIVIDE-BY-TWELVE COUNTERS



NC – No internal connection

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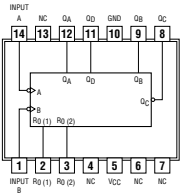
93
4-BIT BINARY COUNTERS



NC – No internal connection

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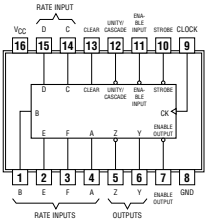
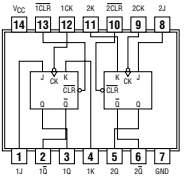
SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIER



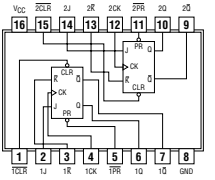
See page 178

107
DUAL J-K FLIP-FLOPS WITH CLEAR



See page 180

109
DUAL J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR



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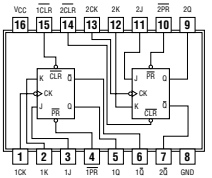
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR



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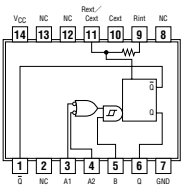
MONOSTABLE MULTIVIBRATOR



NC – No internal connection

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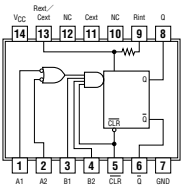
122

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR



NC – No internal connection

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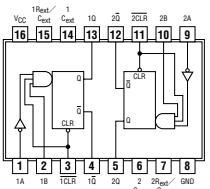
123

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBARATORS WITH CLEAR



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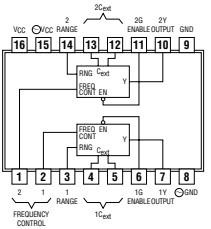
124

DUAL VOLTAGE-CONTROLLED OSCILLATORS WITH ENABLE INPUTS



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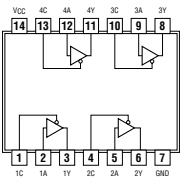
QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

positive logic:

Y = A



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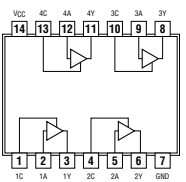
126

QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

positive logic:

Y = A



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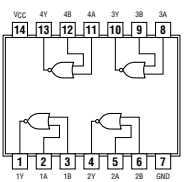
128

SN54128...75-Ω LINE DRIVER
SN74128...50-Ω LINE DRIVER

positive logic:

Y = $\overline{A + B}$



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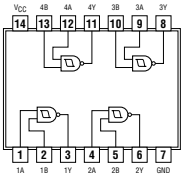
132

QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

positive logic:

$Y = \overline{A \cdot B}$



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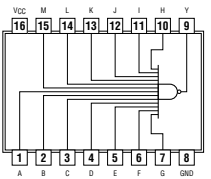
133

13-INPUT POSITIVE-NAND GATES

positive logic:

$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M}$



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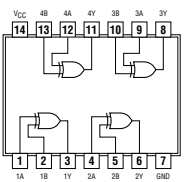
QUAD 2-INPUT EXCLUSIVE-OR GATES WITH OPEN COLLECTOR OUTPUTS

positive logic:

$Y = A \oplus B = \overline{A}B + \overline{A}\overline{B}$



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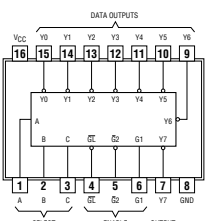
137

3-TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES



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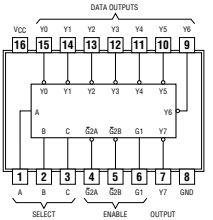
3-TO-LINE DECODERS/DEMULTIPLEXRS



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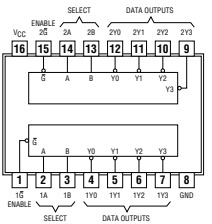
139

DUAL 2-TO-4-LINE DECODERS/DEMULTIPLEXERS



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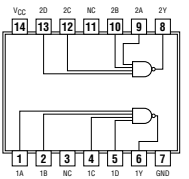
DUAL 4-INPUT POSITIVE-NAND 50-Ω LINE DRIVERS

positive logic:

$Y = \overline{ABCD}$



NC – No internal connection

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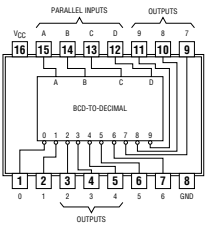
BCD-TO-DECIMAL DECODERS/DRIVERS FOR LAMPS, RELAYS, MOS



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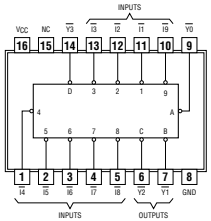
Pin Assignments

147
10-TO-4 LINE PRIORITY ENCODER



NC – No internal connection

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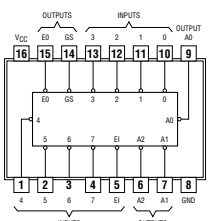
148
8-TO-3-LINE OCTAL PRIORITY ENCODERS



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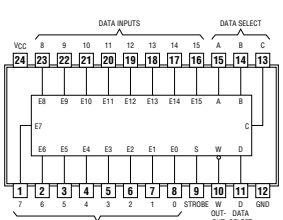
150
1-OF-16 DATA SELECTOR



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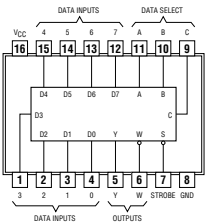
151
8-TO-1 LINE DATA SELECTORS/MULTIPLEXERS



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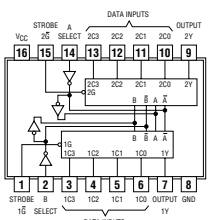
153
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS



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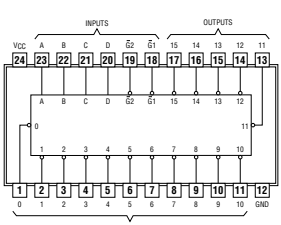
154
4-LINE TO 16-LINE DECODER/DEMULTIPLEXER



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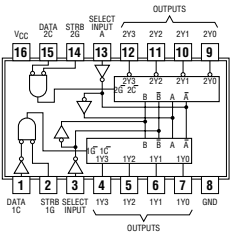
156
DECODERS/DEMULTIPLEXERS



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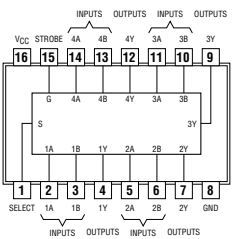
158
QUAD 2-TO 1-LINE DATA SELECTORS/MULTIPLEXERS



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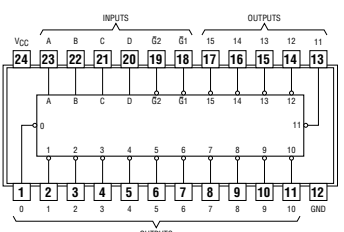
159
4-TO-16 LINE DECODER/DEMULTIPLEXER



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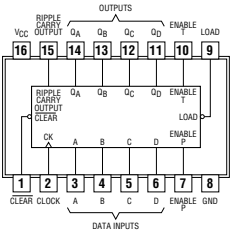
161
163
SYNCHRONOUS 4-BIT BINARY COUNTERS



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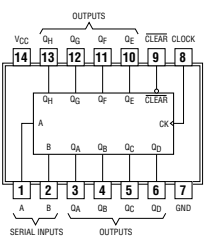
164
8-BIT PARALLEL OUTPUT SERIAL SHIFT REGISTERS



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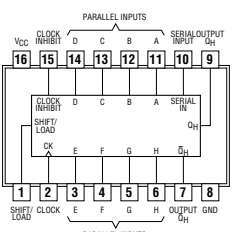
165
8-BIT SHFT REGISTERS



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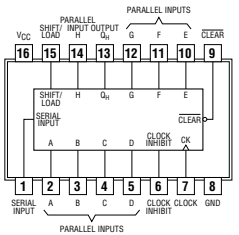
166
8-BIT SHIFT REGISTERS



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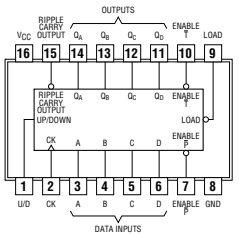
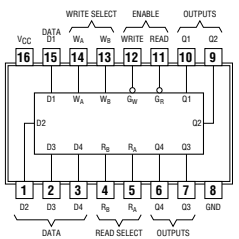
169
4-BIT UP/DOWN SYNCHRONOUS BINARY COUNTERS



See page 234

170
4-BY-4-REGISTER FILES



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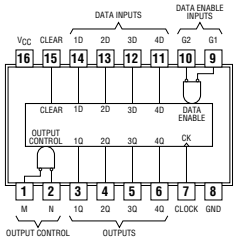
173
4-BIT D-TYPE REGISTERS



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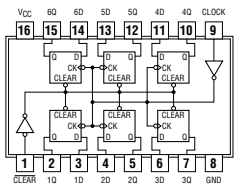
174
HEX D-TYPE FLIP-FLOPS



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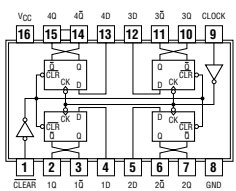
175
QUAD D-TYPE FLIP-FLOPS



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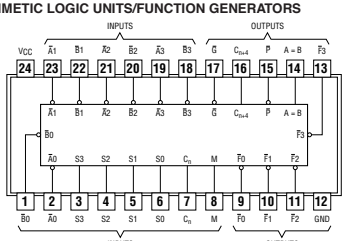
181
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS



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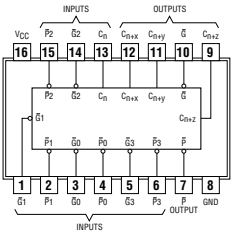
182
LOOK-AHEAD CARRY GENERATORS



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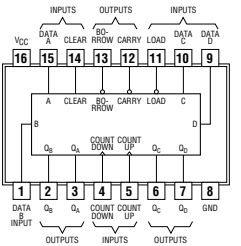
193
SYNCHRONOUS UP/DOWN DUAL CLOCK COUNTERS



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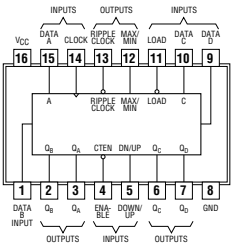
191
SYNCHRONOUS UP/DOWN DUAL CLOCK COUNTERS



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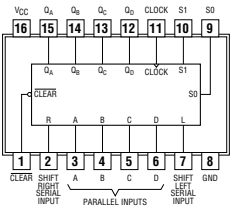
194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS



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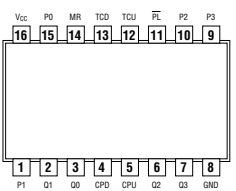
192
PRESETTABLE SYNCHRONOUS 4-BIT UP/DOWN COUNTERS



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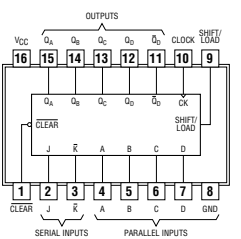
195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS



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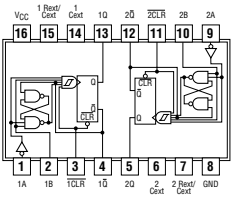
221
DUAL MONOSTABLE MULTIVIBRATORS



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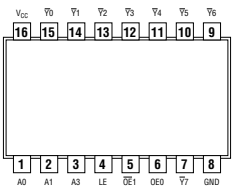
237
3-TO-8 LINE DECODER DEMULTIPLEXER WITH ADDRESS LATCHES



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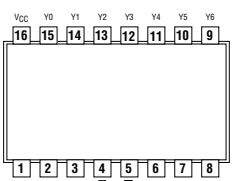
238
3-TO-8-LINE DECODERS/DEMULTIPLEXERS



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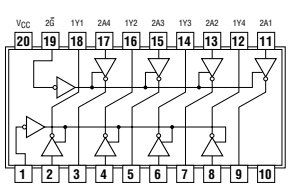
240
OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS



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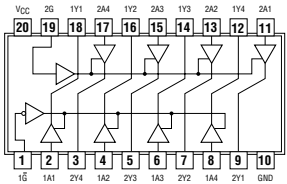
241
OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS



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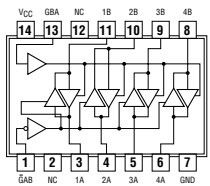
243
QUADRUPLE BUS TRANSCEIVERS



NC – No internal connection

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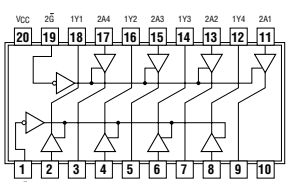
244
OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS



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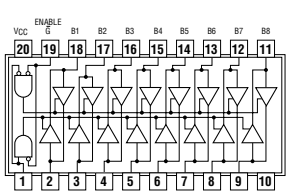
245
OCTAL BUS TRANSCEIVERS



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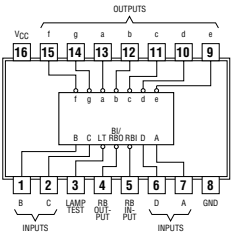
247 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS WITH RIPPLE BLANKING



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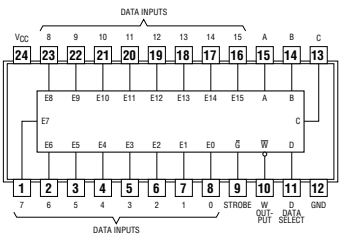
1-OF-16 DATA GENERATOR/MULTIPLEXER



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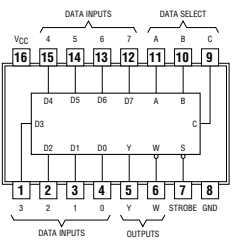
DATA SELECTORS/MULTIPLEXERS



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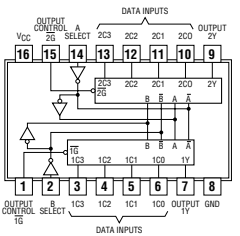
DUAL DATA SELECTORS/MULTIPLEXERS



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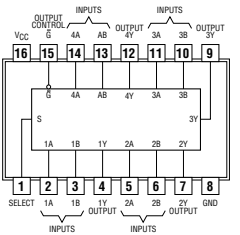
QUAD DATA SELECTORS/MULTIPLEXERS



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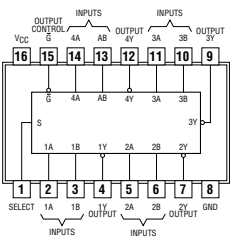
QUAD DATA SELECTORS/MULTIPLEXERS



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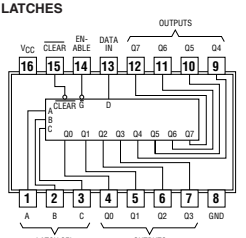
8-BIT ADDRESSABLE LATCHES



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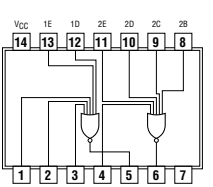
DUAL 5-INPUT POSITIVE-NOR GATES

positive logic:

$Y = A + B + C + D + E$



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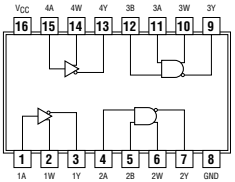
QUAD COMPLEMENTARY-OUTPUT ELEMENTS

positive logic:
$Y = \overline{A}$, $W = A$
$Y = AB$, $W = \overline{AB}$



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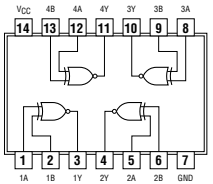
QUAD 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{A \oplus B}$



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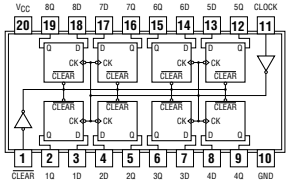
OCTAL D-TYPE FLIP-FLOPS



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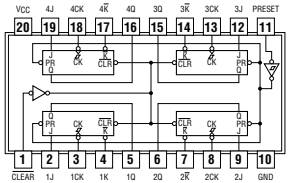
QUAD J-$\overline{K}$ FLIP-FLORS



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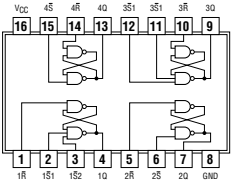
QUAD $\overline{S}$-$\overline{R}$ LATCHES



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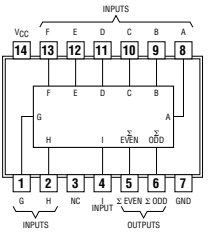
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS



NC – No internal connection

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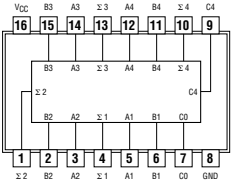
4-BIT BINARY FULL ADDERS



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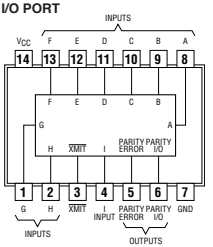
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS WITH BUS DRIVER PARITY I/O PORT



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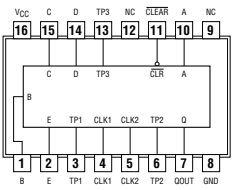
PROGRAMMABLE FREQUENCY DIVIDER/DIGITAL TIMER



NC – No internal connection

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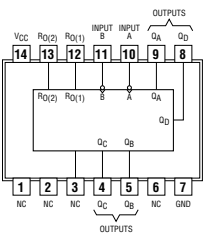
4-BIT BINARY COUNTERS



NC – No internal connection

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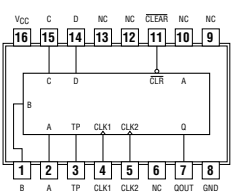
PROGRAMMABLE FREQUENCY DIVIDER/DIGITAL TIMER



NC – No internal connection

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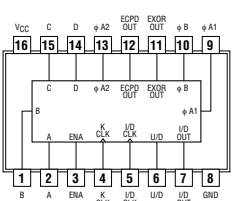
DIGITAL PHASE-LOCKED-LOOP FILTERS



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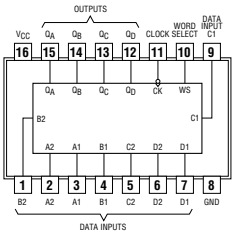
QUAD 2-INPUT MULTIPLEXERS WITH STORAGE



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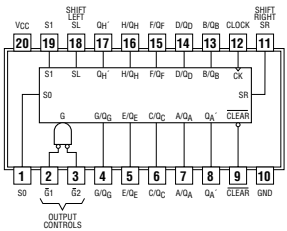
8-BIT BIDIRECTIONAL UNIVERSAL SHIFT/STORAGE REGISTERS



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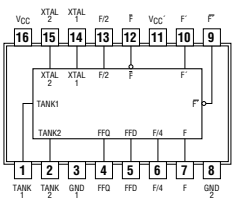
CRYSTAL-CONTROLLED OSCILLATOR



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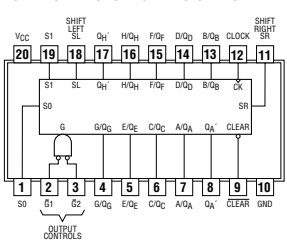
8-BIT BIDIRECTIONAL SHIFT/STORAGE REGISTERS



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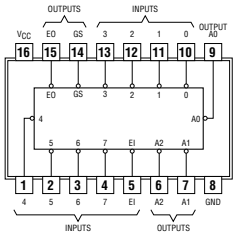
8-LINE TO 3-LINE PRIORITY ENCODER



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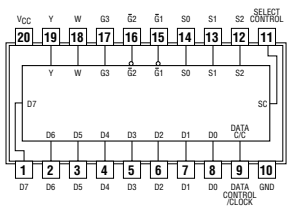
356
8-INPUT MULTIPLEXERS/REGISTERS 3-STATE



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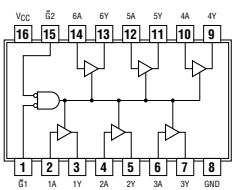
HEX BUS DRIVERS



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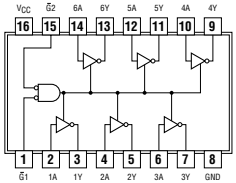
HEX BUS DRIVERS
HEX BUFFERS/LINE DRIVERS 3-STATE



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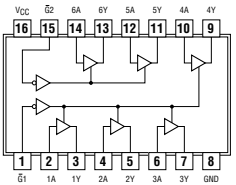
HEX BUS DRIVERS



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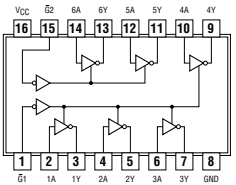
HEX BUS DRIVERS



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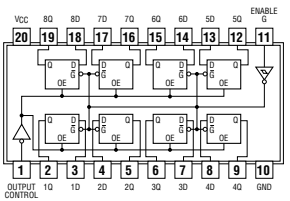
OCTAL D-TYPE LATCHES



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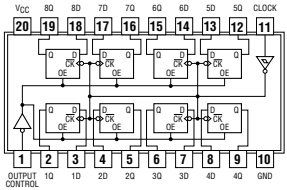
OCTAL D-TYPE FLIP-FLOPS



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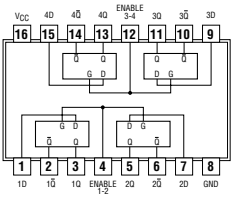
4-BIT BISTABLE LATCHES



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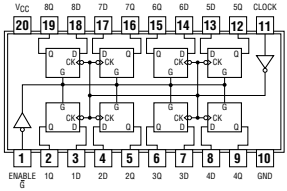
OCTAL D-TYPE FLIP-FLOPS



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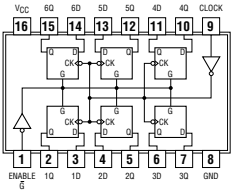
HEX D-TYPE FLIP-FLOPS



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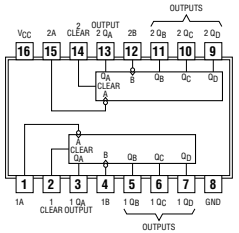
DUAL DECADE COUNTERS



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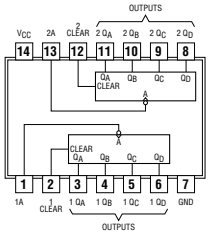
DUAL 4-BIT BINARY COUNTERS



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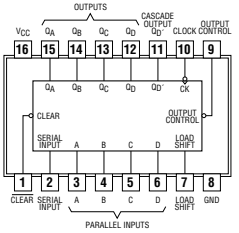
4-BIT UNIVERSAL SHIFT REGISTERS



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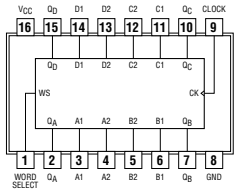
QUAD 2-INPUT MULTIPLEXER WITH STORAGE



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