I2C Overview

- □ Multi-mastered
- □ Send and receive
- □ Two wire (plus ground)
- □ Serial



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Terminology

TERM	DESCRIPTION
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by a master
Multi-master	More than one master can attempt to control the bus at the same time without corrupting the message
Arbitration	Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the winning message is not corrupted
Synchronization	Procedure to synchronize the clock signals of two or more devices

Table 1 Definition of I²C-bus terminology



Fig.3 Connection of Standard- and Fast-mode devices to the I²C-bus.

wired-and configuration

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Interfacing to the Bus



Electrical connection is fine. But the software is complex



Memory mapped device that handles bit level interface. Only do byte level stuff in software

Bit Transfer



Master

Fig.4 Bit transfer on the I²C-bus.

The one who initiates a frame:



Fig.5 START and STOP conditions.

A frame is: <Start><addr><data>...<data><Stop> OR <Start><addr><data>...<data><R_Start><addr><data>...<Stop>

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An I2C Byte Transfer



Fig.6 Data transfer on the I²C-bus.



Fig.10 A complete data transfer.

Addresses are 7 bits, LSB of address byte is Read/Write control. Determines whether master or slave becomes the transmitter

Arbitration



Fig.9 Arbitration procedure of two masters.

It is up to the failed master to try again when the bus is not busy. Seems like high address devices are low priority receivers...but I haven't read this anywhere

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Using the Bus Interface



A0 = HIGH	enables data transfer to/from register S1
A0 = LOW	Access to all other registers defined by the bit pattern in register S1

Loads byte 80H into register S1' i.e. next byte will be loaded into register S0' (own address register); serial interface off.

Loads byte 55H into register S0'; effective own address becomes AAH.

Loads byte A0H into register S1, i.e. next byte will be loaded into the clock control register S2.

Loads byte 1CH into register S2; system clock is 12 MHz; SCL = 90 kHz.

Loads byte C1H into register S1; register enable serial interface, set I²C-bus into idle mode; SDA and SCL are HIGH. The next write or read operation will be to/from data transfer register S0 if A0 = LOW.

On power-on, if an PCF8584 node is powered-up slightly after another node has already begun an I²C-bus transmission, the bus busy condition will not have been detected. Thus, introducing this delay will insure that this condition will not occur.

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Slave Flow



Slave Receiver Mode

