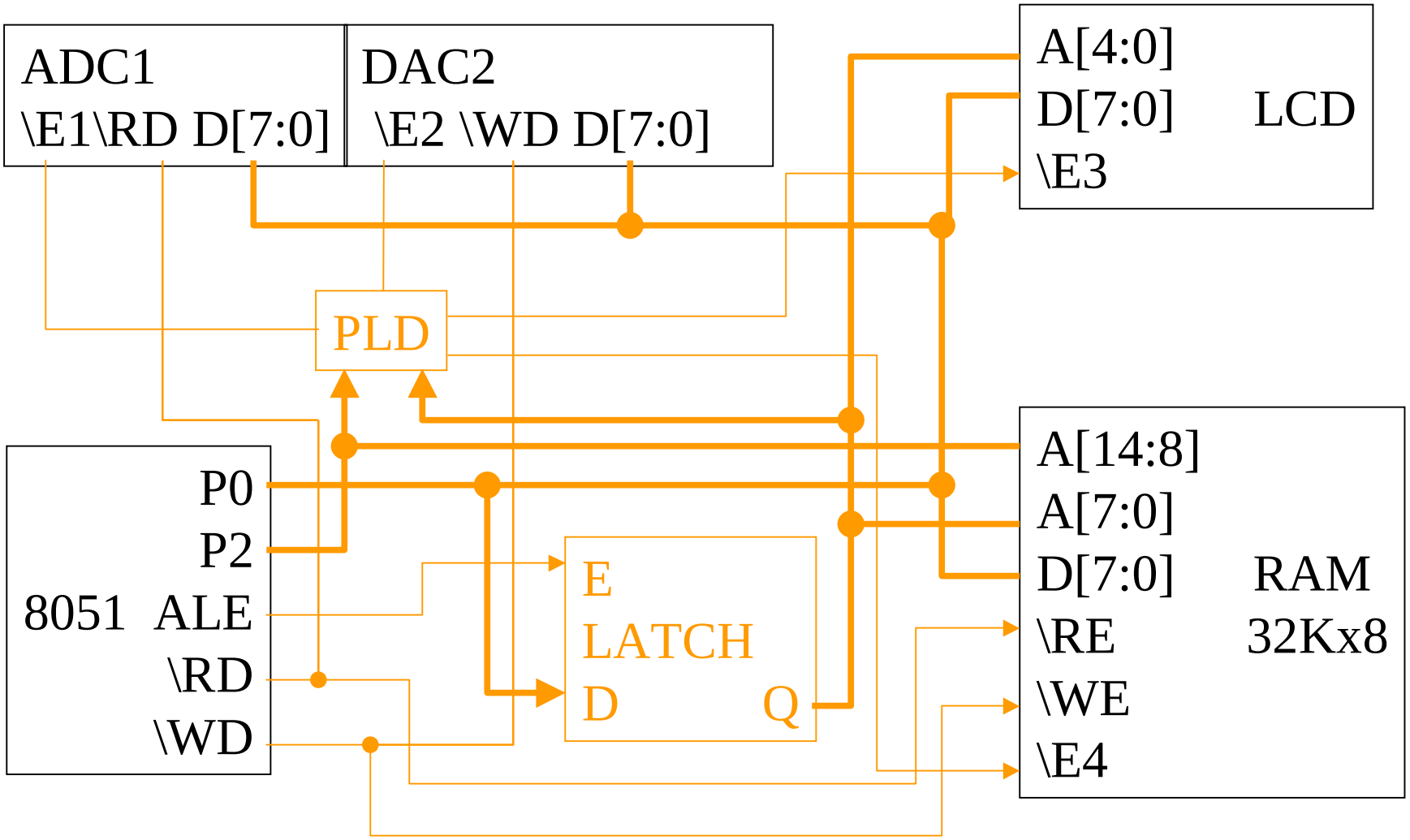
What's Coming

- Hardware
  - Basic Filters and Noise Management
  - Serial Communications
- Design Meeting
- Move the quiz up to Monday 10/16 from 10/20.

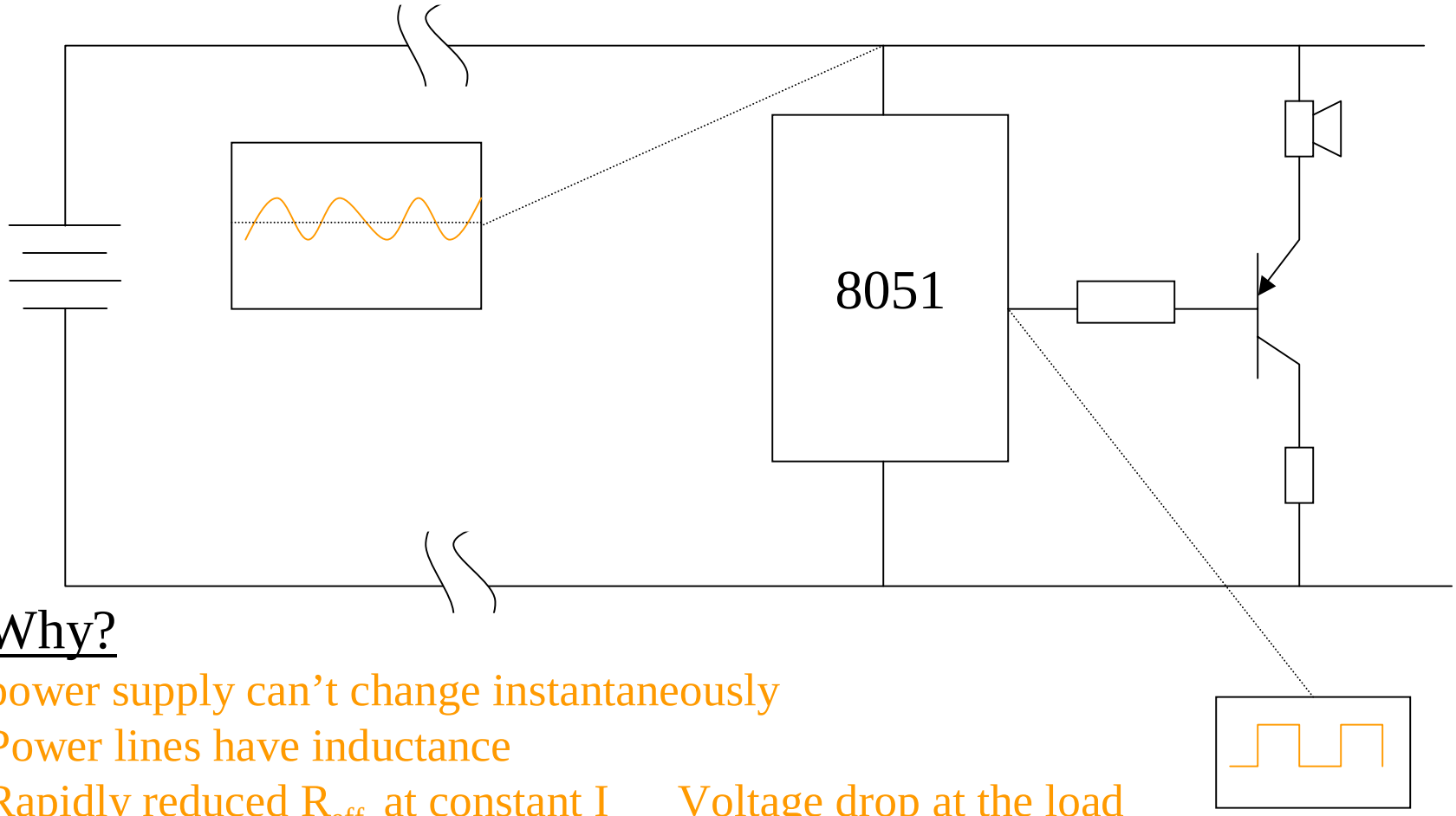
Example


ADC1
\E1\RD D[7:0]
DAC2
\E2 \WD D[7:0]
A[4:0]
D[7:0]
\E3
LCD
PLD
P0
P2
8051 ALE
\RD
\WD
E
LATCH
D
Q
A[14:8]
A[7:0]
D[7:0]
\RE
\WE
\E4
RAM
32Kx8

Address Decoder Logic Design

1. Define External Memory Map (64K): addr[15:0]
   Ram: Upper 32K enable if address = 1xxxxxxxxxxxxxxx
   LCD: 0-31 enable if address = 0xxxxxxxx00xxxxx
   DAC2: 32 enable if address = 0xxxxxxxx01xxxxx
   ADC1: 64 enable if address = 0xxxxxxxx10xxxxx
2. Come up w/ address decoder logic for each case (many to 1 ok, 1 to many not okay!)
   \E4 = (A15)' covers all upper 32K addresses
   \E3 = (A15'A6'A5')' covers 2^12 addresses including 0-31 but excluding upper 32K, 64, 32
   \E2 = (A15'A6'A5)' covers 2^13 addresses but excludes upper 32K, 64, 0-31
   \E1 = (A15'A6A5')' covers 2^13 addresses but excludes upper 32K, 32, 0-31

Power Supply Noise



Why?

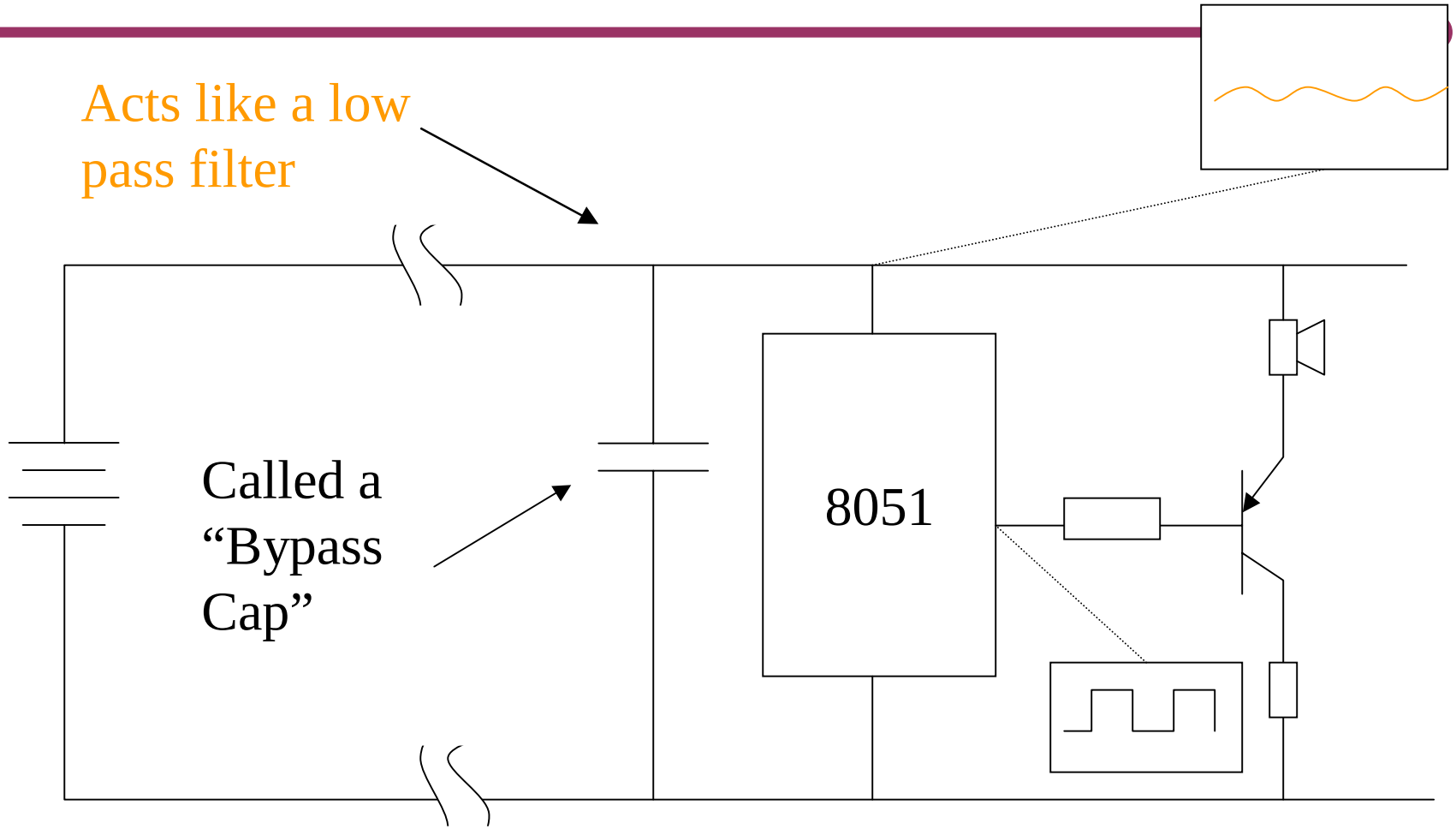
power supply can't change instantaneously

Power lines have inductance

Rapidly reduced R_{eff} at constant I Voltage drop at the load

So what? Could cause processor to reset/go to unknown state, mess up analog voltage readings, cause electromagnetic interference

What to do about it?



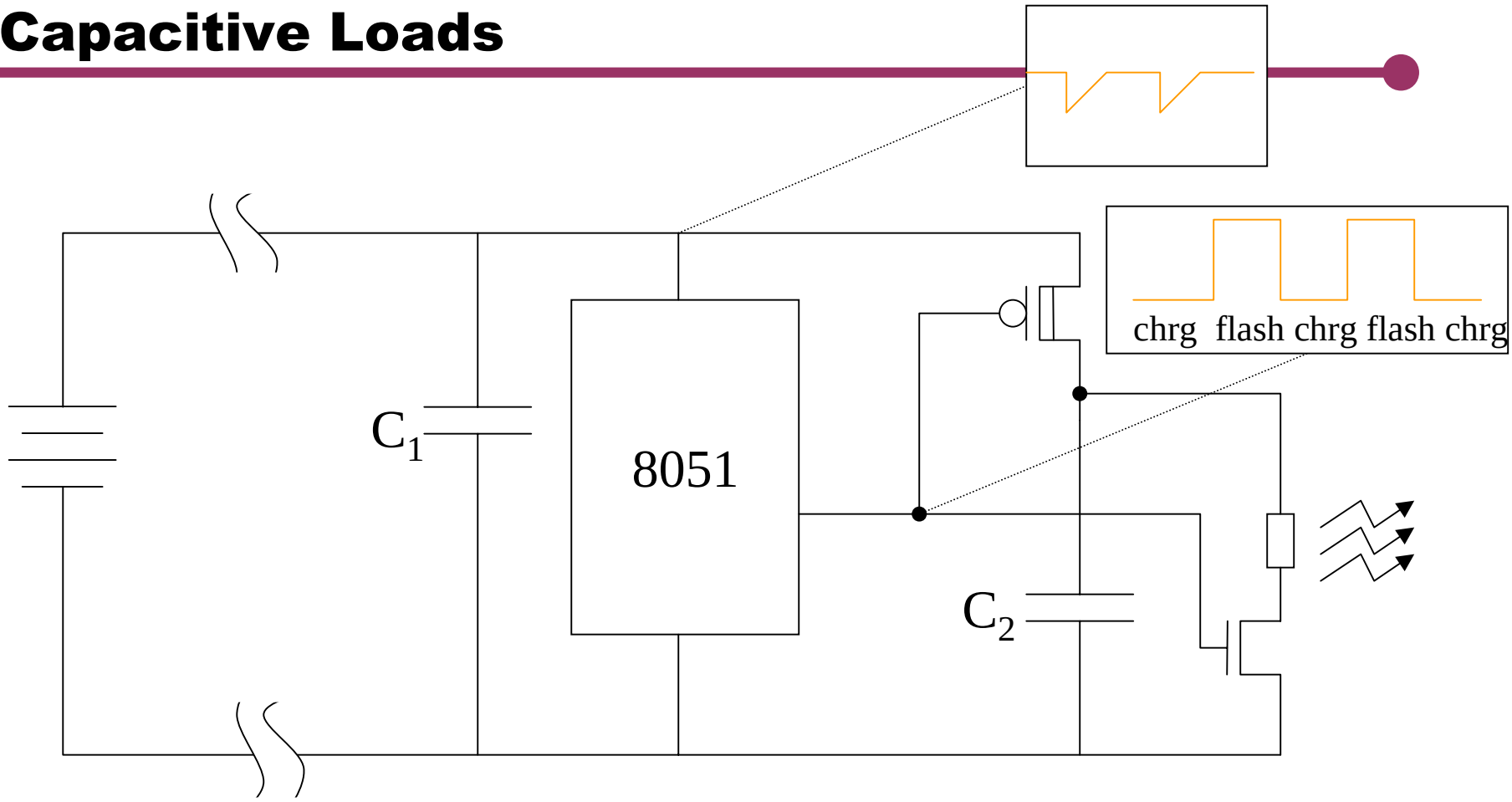
How big should cap be?

Depends on speed and inductance of the supply, and ΔI when switched

Typical values for digital boards are .1uF/IC placed very close to IC

….then there's capacitive loads….

Capacitive Loads



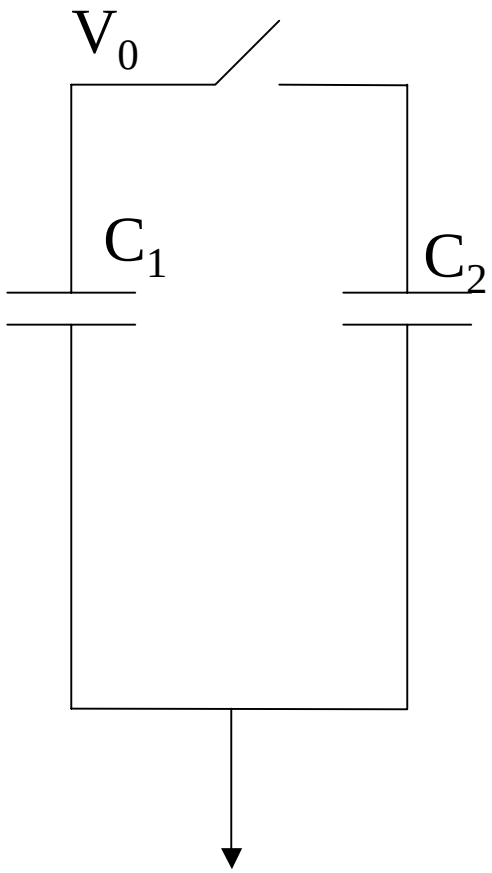
Why is this worse than resistive load?

Recharge current is only limited by available electrons!

Can cause massive voltage drop until battery catches up.

So what? Last year's capstone project: sonar firing caused processor reset

Charge Sharing

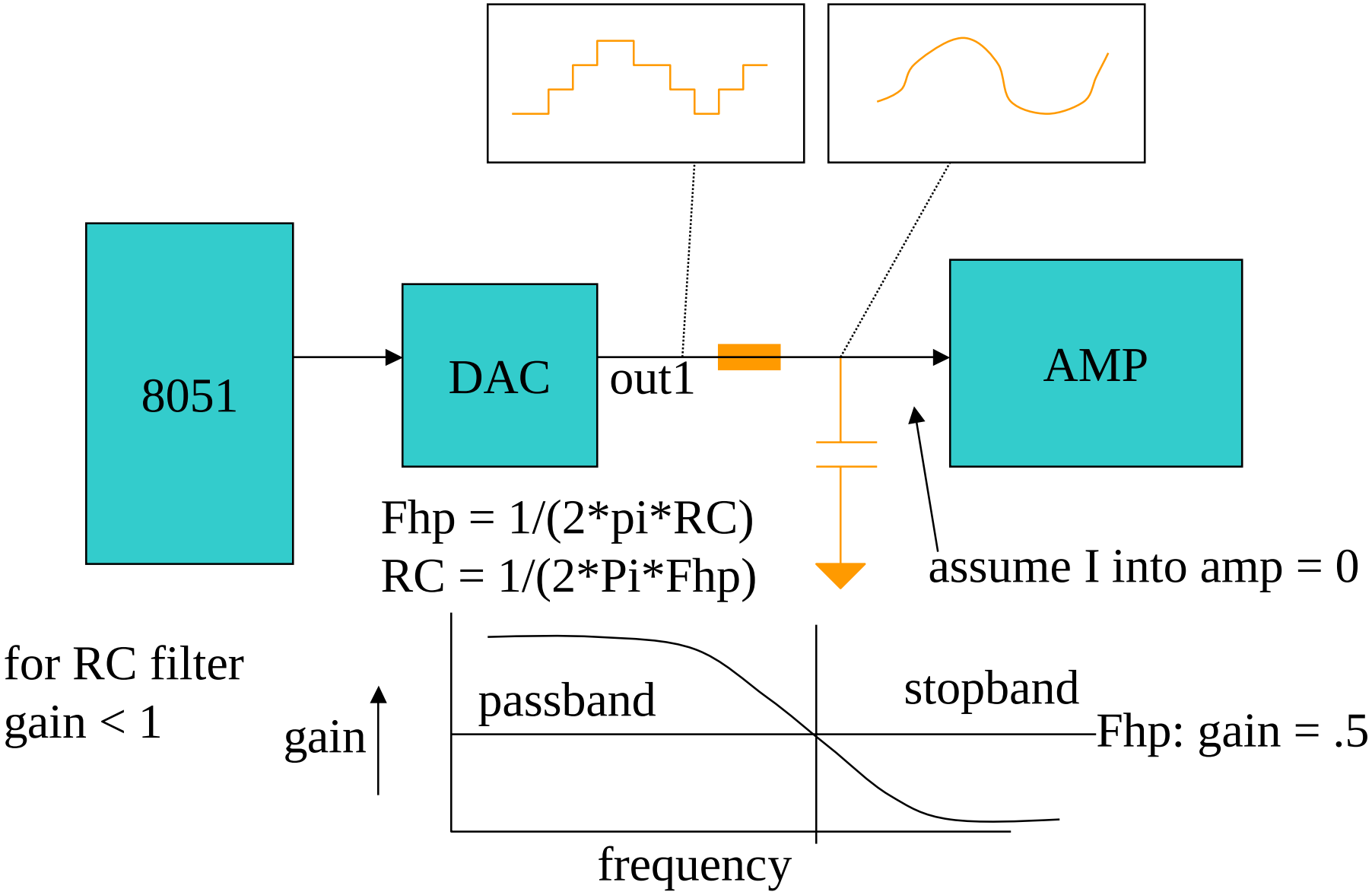


1. Initially $Q_1=V_0C_1$
2. Then close switch, what is V'/V_0 ?
3. **$V_0 = Q_1/C_1$ (initial condition)**
4. **$Q_1'+Q_2' = Q_1$ (post condition)**
5. $Q_1 = V'C_1+V'C_2 = V'(C_1+C_2)$
6. $V' = Q_1/(C_1+C_2)$
7. $V'/V0 = Q_1/(C_1+C_2) * C_1/Q_1$
8. $V'/V_0 = C_1/(C_1+C_2)$

If C_1 dominates, then $V' \sim V_0$

If $C_1 = 10C_2$ Then $V_1/V_0 = 10/11$

Where else could we use a low pass filter?

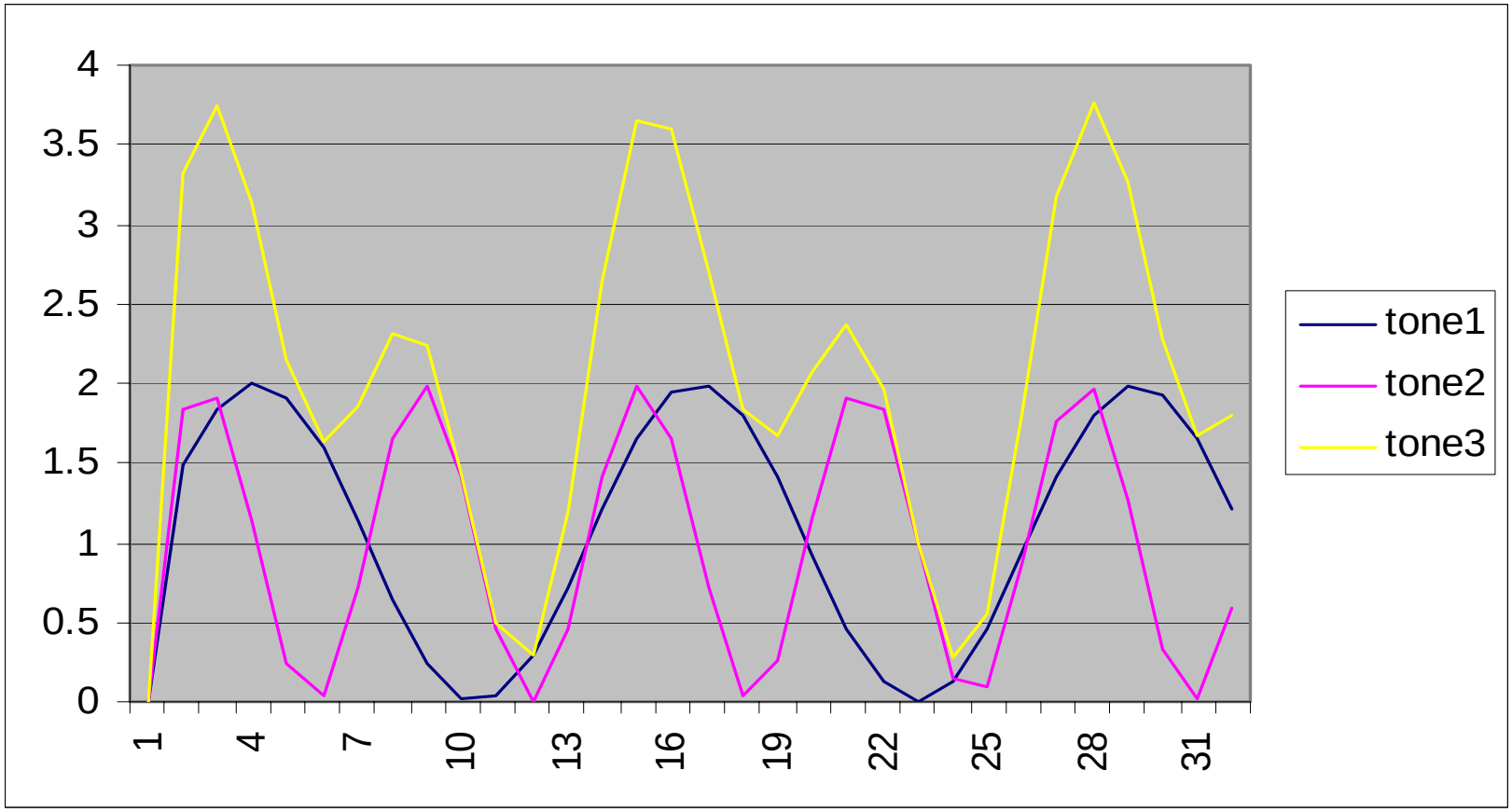


Design Meeting

- We can play tones.
- What do we have to do now?
  - Music representation – what is music?
  - Basic I/O to the host (PC)
  - C
  - Multiple independent tones with a single timer

Is Constant Rate Sampling Okay?

- Just like CD player: runs a 44KHz…max frequency it can create is 22KHz,
- A CD recording of a pure 22HKz tone would look like a square/triangle wave on the output of the DAC.



two frequencies with same rate. How fast can you go?

Frequency range w/ fixed sample rate

To get a psuedo-sine wave, what is the max Stride for our lookup table?

- 64: 64/156 (5K) = 1.125KHz

Let Stride = 1 and Sample Rate = 5KHz

- output frequency = 5KHz/256 = 19.531Hz
- low frequencies generate a smoother waveform

Let Stride = n

- output frequency = 5KHz/(256/n) = n*(5KHz/256)

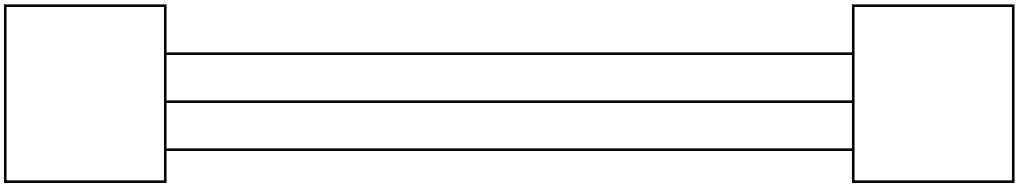
Solve for output frequency

- Stride = (freq*256)/5KHz
- Middle C = 262Hz, so stride = 13.41 can we just round this off? Yes for this week's lab.
- D = 294, so stride = 15.05

What happens for low frequencies

- Low F: 87.31Hz stride = 4.74
- Low E: 82.42Hz stride = 4.47
- what do we do with non-integral strides?

Serial Communication: RS-232 (IEEE Standard)



- Serial protocol for point-to-point low-cost, low speed applications
- Commonly used to connect PCs to I/O devices
- RS-232 wires

TxD -- transmit data
TxC -- transmit clock
RTS – request to send
CTS – clear to send

RxD – receive data
RxC – receive clock
DSR – data set ready :
DTR – data terminal ready

SG -- Signal Ground

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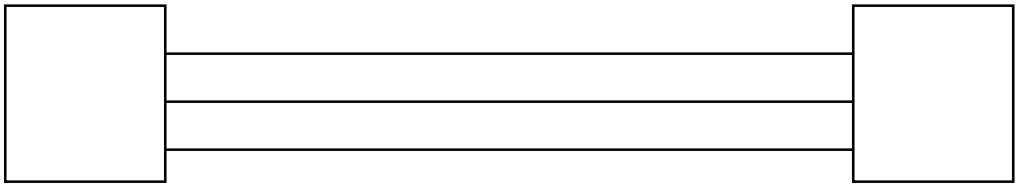
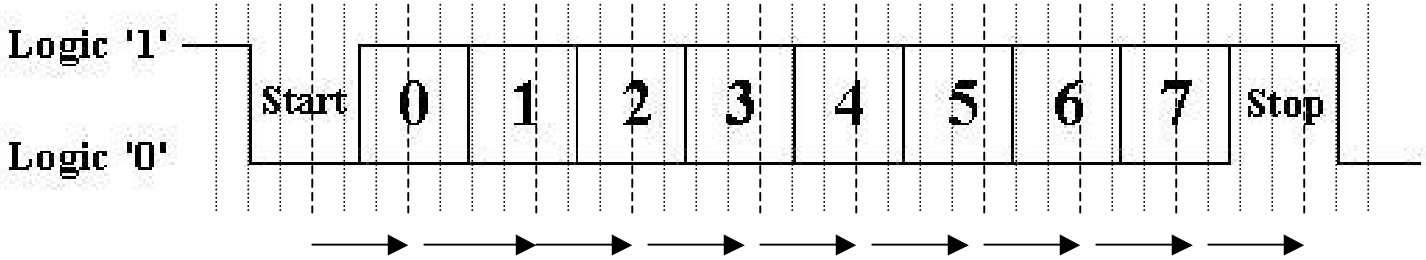
Transfer modes

- Synchronous
  - Clock signal wire is used by both receiver and sender to sample data
- Asynchronous
  - No clock signal in common
  - Data must be over-sampled
  - Needs only three wires (one data for each direction, and ground)
- Flow control
  - Handshaking signals to control byte rate, not bit rate
  - Optional

Data Format



Start Bit, Stop bit , Data bits, Parity Bit (odd, even, none)

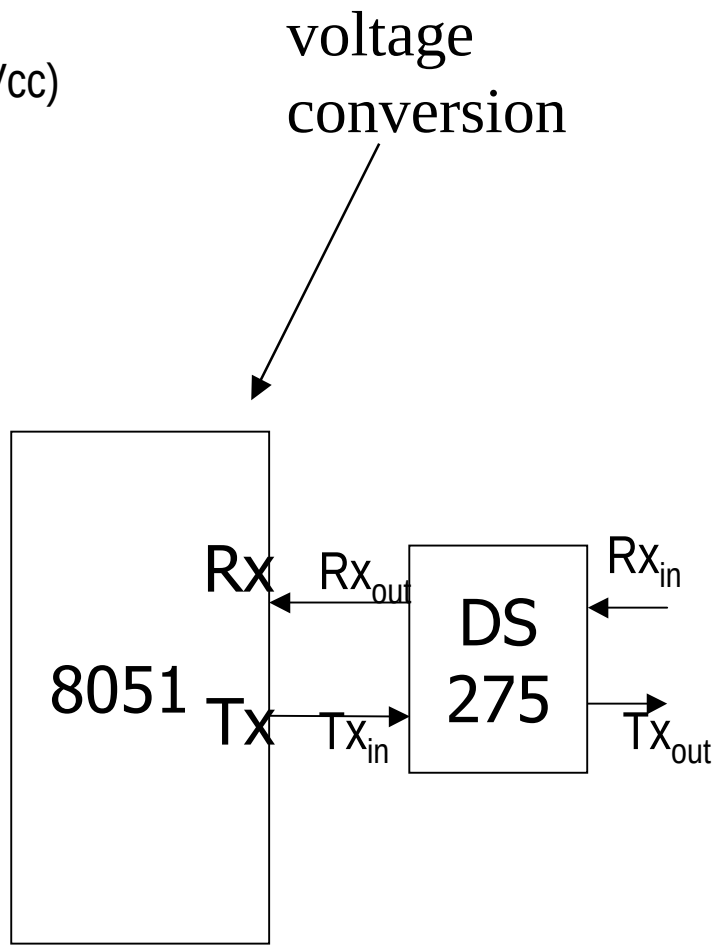


- Logic 0 (space): between +3 and +25 Volts.
- Logic 1 (mark): between -3 and -25 Volts.
- Undefined between +3 and -3 volts.

Level Converter: DS 275

- Pin Description

RXout	- RS- 232 Receiver Output (-0.3V to Vcc)
Vdrv	**- Transmit driver +V (hook to Vcc)**
TXin	- RS-232 Driver Output (-0.3V to Vcc)
GND	- System ground
TXout	- RS-232 Driver Output (+/- 15 V)
RXin	- RS-232 Receive Input (+/- 15 V)
Vcc	- System Logic Supply (+5V)



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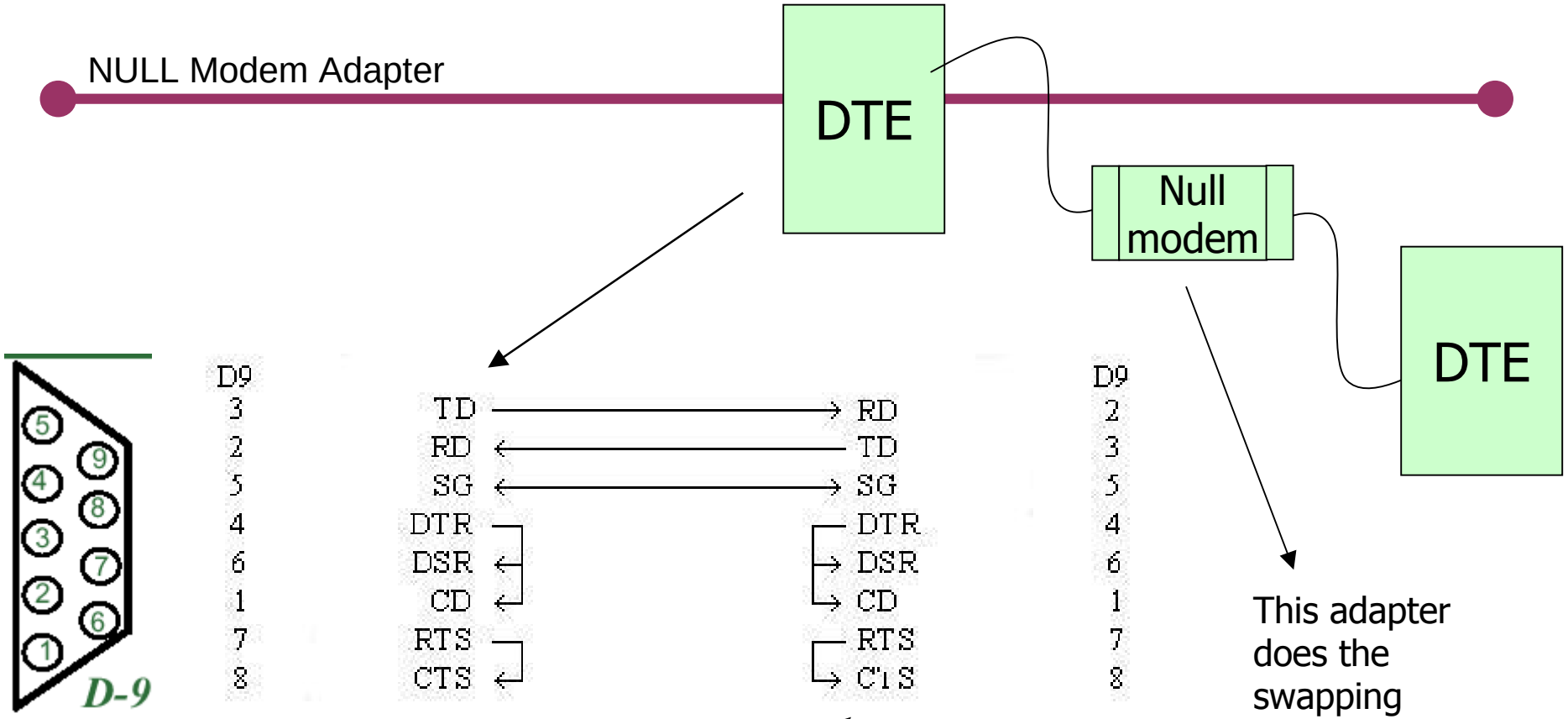
NULL Modem Adapter



- Using only TD, RD, and SG
- No need for flow control (May miss characters if sent too fast)
- Both ends ready to send/receive at any time