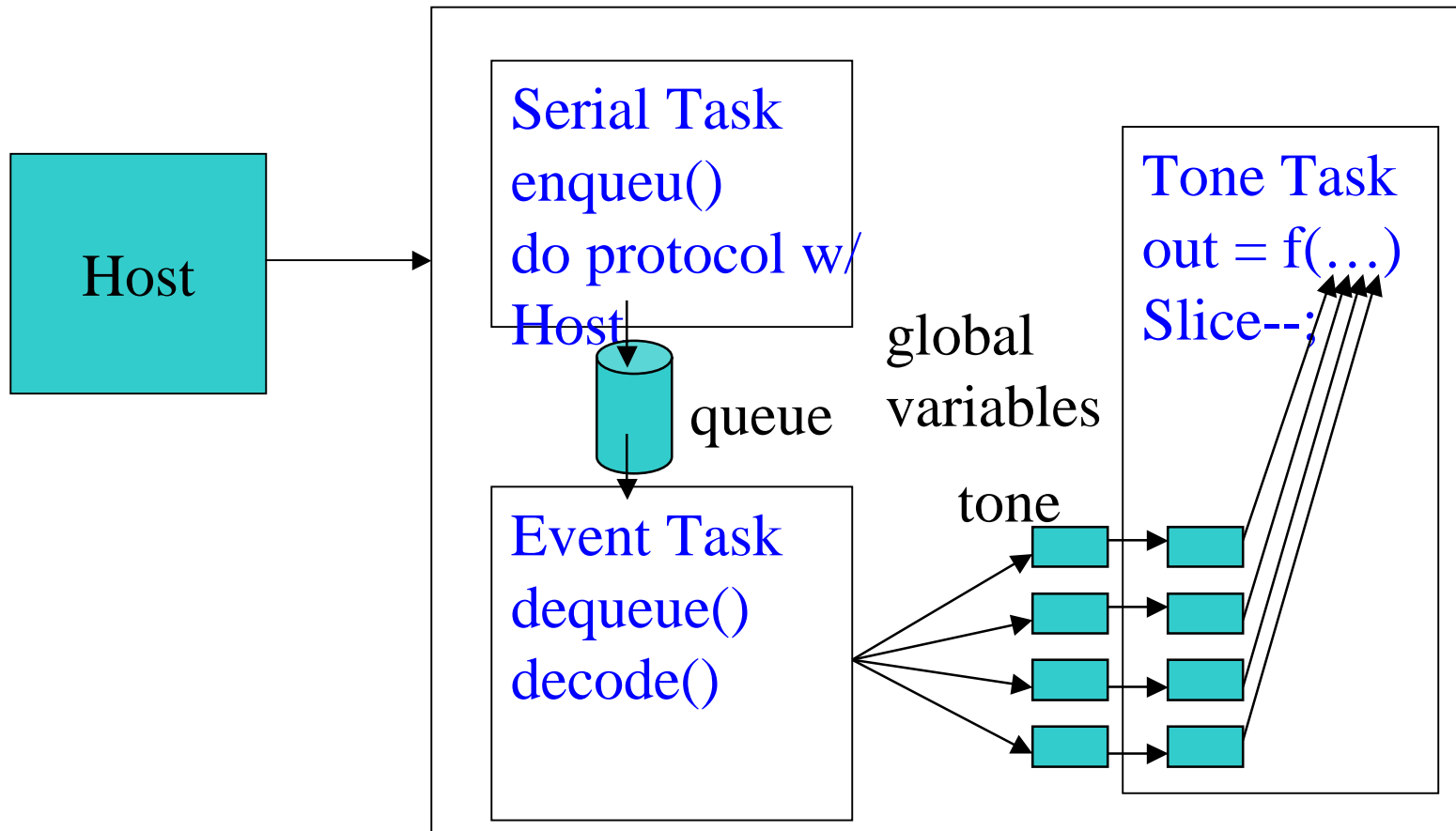


# Music Format

1	5	2	6	2
p	tne	chan	note	amp

if amp = 0, note is a command  
switch(note)  
0: turn off specified channel  
1: continue for specified tne w/ no change  
else  
set specified channel to specified  
note at specified amplitude (1-3)

# Data Rate



Worst Case Data Rate: 4 simultaneous packets/event = 8 bytes/event  
at 200events/sec \* 8bytes/event = 1600bytes/sec = 12.8Kbps  
can we run at 19.2?

# Serial Communication: RS-232 (IEEE Standard)

- n Serial protocol for point-to-point low-cost, low speed applications
- n Commonly used to connect PCs to I/O devices
- n RS-232 wires

TxD -- transmit data

TxC -- transmit clock

RTS – request to send

CTS – clear to send

RxD – receive data

RxC – receive clock

DSR – data set ready :

DTR – data terminal ready

SG -- Signal Ground

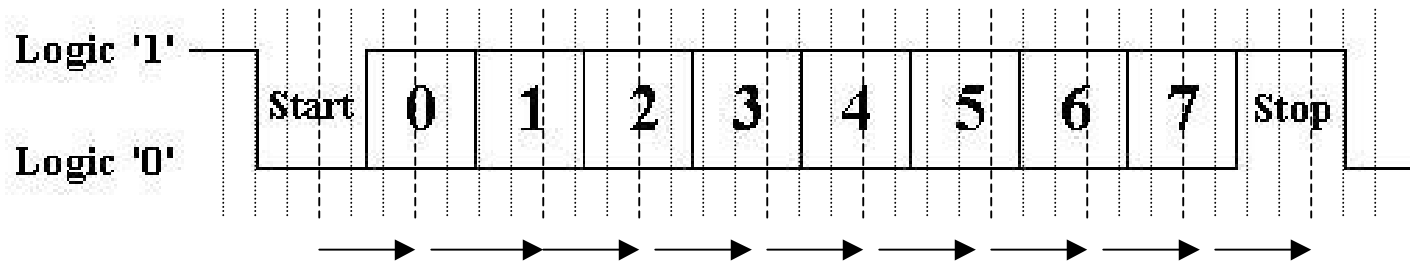
# Transfer modes

---

- q Synchronous
  - Clock signal wire is used by both receiver and sender to sample data
- q (Pseudo) Asynchronous
  - No clock signal in common
  - Data must be over sampled to “synchronize”
  - Needs only three wires (one data for each direction, and ground)
- q Flow control
  - Handshaking signals to control byte rate, not bit rate. Signals like RTS, CTS, DSR, DTR
  - optional

## Data Format

Start Bit, Stop bit , Data bits, Parity Bit (odd, even, none)

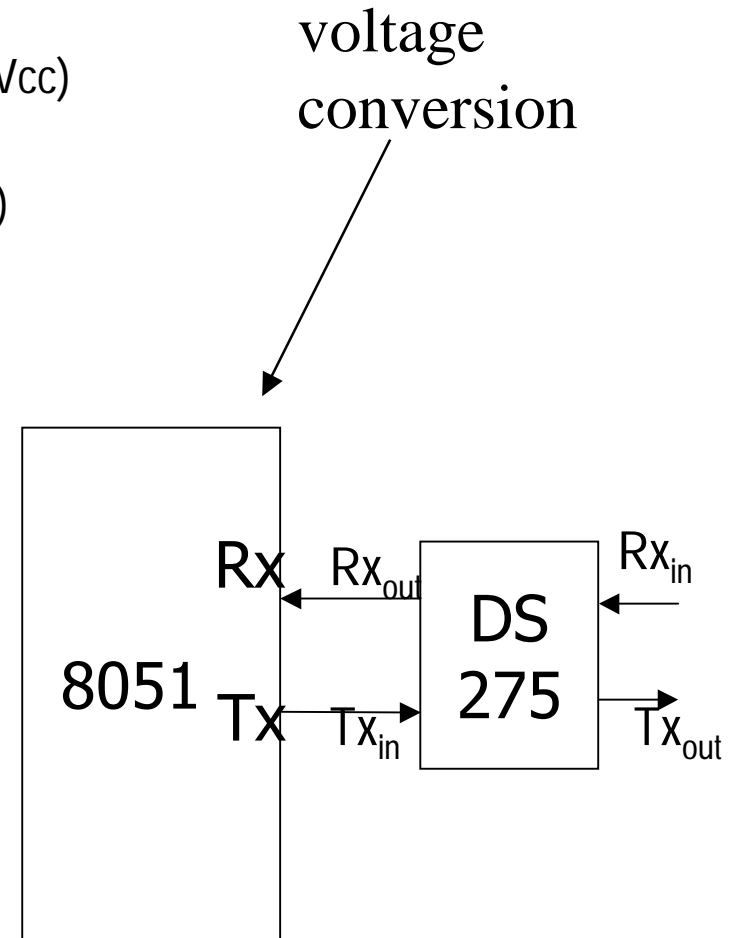


- q Logic 0 (space): between +3 and +25 Volts.
- q Logic 1 (mark): between -3 and -25 Volts.
- q Undefined between +3 and -3 volts.

## Level Converter: DS 275

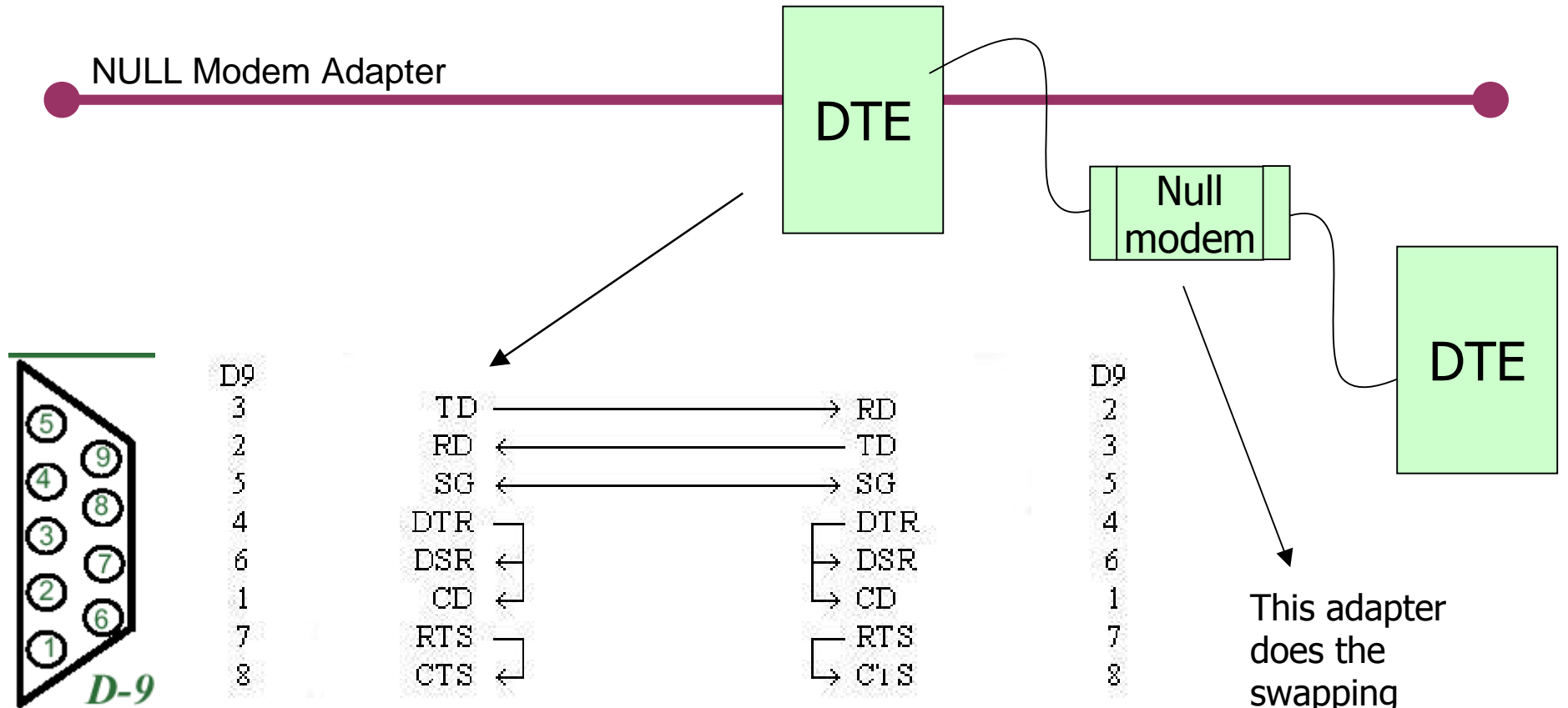
### q Pin Description

- RXout - RS-232 Receiver Output (-0.3V to Vcc)
- Vdrv** - **Transmit driver +V (hook to Vcc)**
- TXin - RS-232 Driver Output (-0.3V to Vcc)
- GND - System ground
- TXout - RS-232 Driver Output (+/- 15 V)
- RXin - RS-232 Receive Input (+/- 15 V)
- Vcc - System Logic Supply (+5V)



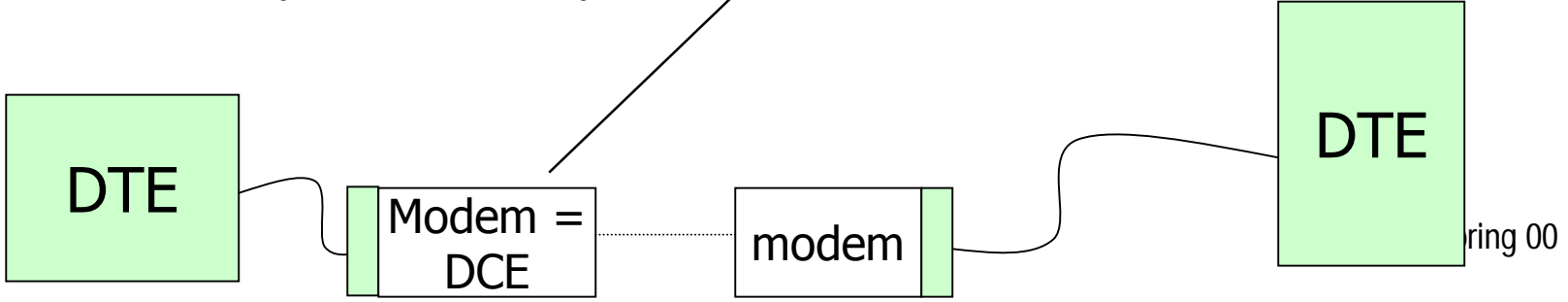
CSE477 -Autumn 99

# NULL Modem Adapter

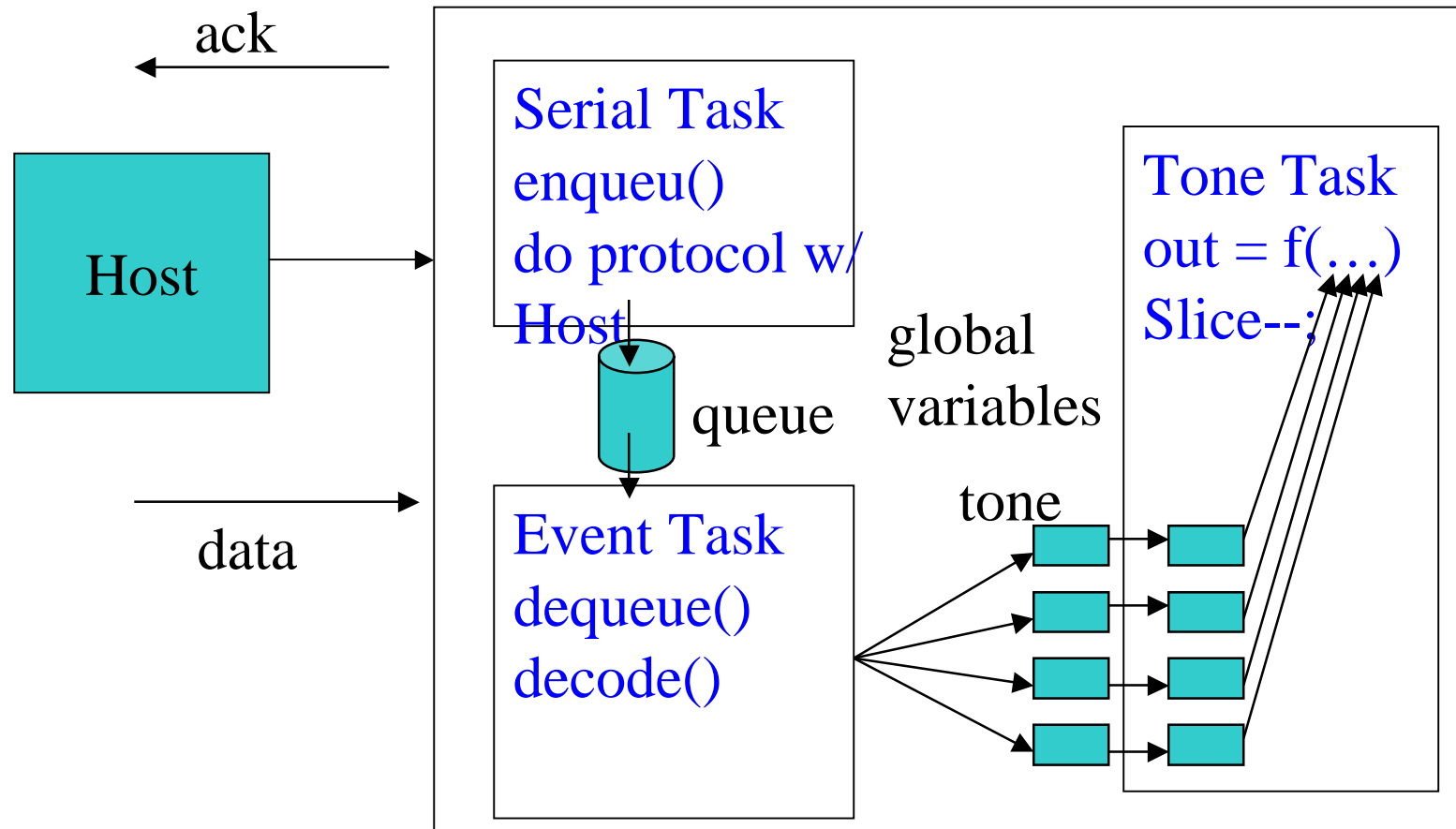


This adapter does the swapping for you.

- q Using only TD, RD, and SG
- q No need for flow control (May miss characters if sent too fast)
- q Both ends ready to send/receive at any time



# SW Flow Control Protocol



Worst Case Data Rate: 4 simultaneous packets/event = 8 bytes/event  
at 200events/sec \* 8bytes/event = 1600bytes/sec = 12.8Kbps  
What determines our true bit rate for keeping the buffer full?



# Review Questions?

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# Comparison Non OS Architectures

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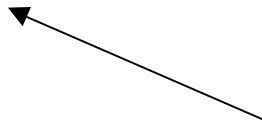
q See Chapter 5, table 5.1 Simon

# Real Time Operating Systems

- q What is the basic thing we want the OS to do to help us improve worst case latency? **Enable multithreading**
- q How? **Define an OS time-slice (tick) at which highest priority 'runnable' task is continued. Priority function determines response behavior.**
- q **Simplest Scheduling algorithm: each task gets at most 1 tick at a time to run. Round Robin Scheduling. Worst case task latency = #tasks\*tick. Worst case run time = ticks/task \* #tasks**
- q **Some properties of such system: liveness, safety, fairness, latency, overhead.**
- q **Other niceties: Device Drivers, Synchronization, Message passing, Memory Management**

# Programmers View

```
void tone_isr(void) interrupt ... {
    process_tones();
    if (!--sliceCount) {
        updateToneParameters();
        sliceCount = SliceSize;
        isr_send_signal(MUSIC);
    }
}
void serial_isr(void) interrupt ...{
    timeCritical();
    os_send_signal(SERIAL);
}
void play(void) _task_ MUSIC {
    os_create(SERIAL);
    while (1) {os_wait();
        process_next_event();}
}
void serial(void) _task_ SERIAL {
    while (1) {os_wait();
        process_serial_data();} // os_create(MUSIC)?
}
```



Tasks are threads

Advantages:

- Deterministic response time even w/ non deterministic tasks lengths.
- Incremental development

Resources:

- Task switching overhead
- Memory overhead
- Use of system timer
- Degrades best case response time.

# Another Solution

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- q Multiprocessor: Dedicate one processor to each (or a few) tasks.
- q Still need **synchronization** and **communication**.
- q A network of M-BOXes could be an example of a multiprocessor system

# Basic Architecture of an RT OS

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- q Task Table
  - Process state, signal flag, time\_out counter, context
- q System Interrupt Service Routine (timer)
- q System Calls (Code, time)

# Embedded Software

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- q Software States v. Finite State Machines
- q Hierarchical State
- q Thread/Process Communication
  - Critical Sections
  - Synchronization
  - Messaging and Signaling