

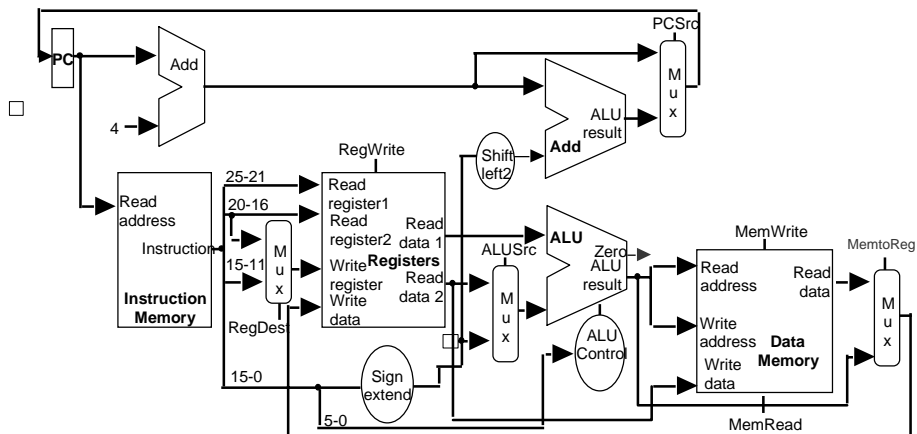


Controlling The Data Path

Control signals must be generated from the instructions to control the behavior of the data path components.

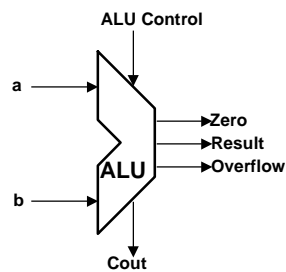
Datapath Schematic

Control lines determine the operation of the datapath components



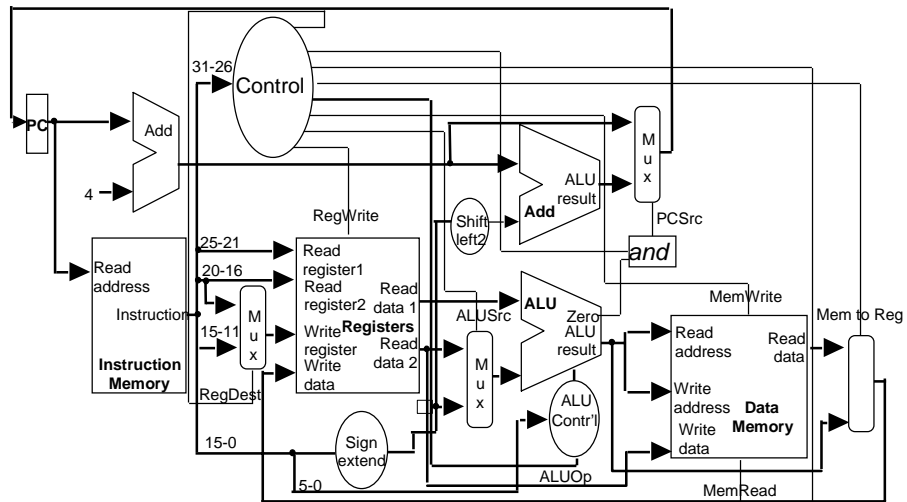
Controlling the ALU

Opcode	ALUOp	Funct	ALU Action	ALU Cnt'l
lw	00	XXXXX	add	010
sw	00	XXXXX	add	010
beq	01	XXXXX	subtract	110
add	10	100000	add	010
subtract	10	100010	subtract	110
and	10	100100	and	000
or	10	100101	or	001
slt	10	101010	set-on-lt	111



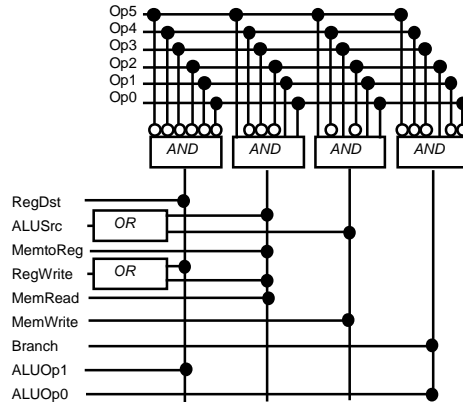
Datapath Control

Control logic is generated from the opcode bits



Computing the Control

Signal	R-type	lw	sw	beq
Op5	0	1	1	0
Op4	0	0	0	0
Op3	0	0	1	0
Op2	0	0	0	1
Op1	0	1	1	0
Op0	0	1	1	0
RegDest	1	0	X	X
ALUSrc	0	1	1	0
MemtoReg	0	1	X	X
RegWrite	1	1	0	0
MemRead	0	1	0	0
MemWrite	0	0	1	0
Branch	0	0	0	1
ALUOp1	1	0	0	0
ALUOp0	0	0	0	1



Computing the Cycle Time

Suppose the following times apply ...

Memory units: 10ns

ALU and adders: 10ns

Register file ref: 5ns

All other operations are 0ns.

Charges for instructions are ...

R-format: 30ns

Load inst: 40ns

Store inst: 35ns

Branch: 25ns

Jump: 10ns

Instruction Mix GCC

22%	Load
11%	Store
49%	R-type
16%	Branch
2%	Jump

$$\text{CPU Clock Cycle} = 40 \times 0.22 + 35 \times 0.11 + 30 \times 0.49 + 25 \times 0.16 + 10 \times 0.02 = 31.6$$

$$\text{CPU Perf}/\text{CPU Perfs} = 40/31.6 = 1.27$$