Read Harris & Harris (1st edition) 7.5 - Pipelined Processor

Q1) From exercise 7.24 from Harris & Harris (1st edition)

The pipelined MIPS processor as covered in section 7.5 is running the following program:

```
add $s0, $t0, $t1
sub $s1, $t2, $t3
and $s2, $s0, $s1
or $s3, $t4, $t5
slt $s4, $s2, $s3
```

Which registers are being written, and which are being read on the 5th cycle (1st instruction is fetched at cycle 1)? Please explain your reasoning with a pipeline table. The table will have a column per pipeline stage (IF, ID, EX, MEM, WB) and a row per cycle. You can label the instructions i1 to i5. If there are pipeline stalls or data forwarding, please indicate those using labels and/or arrows.

<table>
<thead>
<tr>
<th>Cycle</th>
<th>i1</th>
<th>i2</th>
<th>i3</th>
<th>i4</th>
<th>i5</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IF</td>
<td>IF</td>
<td>IF</td>
<td>ID</td>
<td>ID</td>
</tr>
<tr>
<td>2</td>
<td>ID</td>
<td>ID</td>
<td>ID</td>
<td>EX</td>
<td>EX</td>
</tr>
<tr>
<td>3</td>
<td>EX</td>
<td>EX</td>
<td>EX</td>
<td>MEM</td>
<td>MEM</td>
</tr>
<tr>
<td>4</td>
<td>MEM</td>
<td>MEM</td>
<td>MEM</td>
<td>WB</td>
<td>WB</td>
</tr>
<tr>
<td>5</td>
<td>WB</td>
<td>WB</td>
<td>WB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

If there are pipeline stalls or data forwarding, please indicate those using labels and/or arrows.
Q2) Consider the following code:

\[
a = b + e;
\]
\[
c = b + f;
\]

Here is the generated MIPS code for this segment, assuming all variables are in memory and are addressable as offsets from $t0:

\[
lw \ $t1, \ 0($t0) \quad \# \ b \ is \ stored \ at \ 0 \ offset \ from \ $t0
\]
\[
lw \ $t2, \ 4($t0) \quad \# \ Word \ size \ is \ 4 \ bytes \ in \ MIPS
\]
\[
add \ $t3, \ $t1, \ $t2
\]
\[
sw \ $t3, \ 12($t0)
\]
\[
lw \ $t4, \ 8($t0)
\]
\[
add \ $t5, \ $t1, \ $t4
\]
\[
sw \ $t5, \ 16($t0)
\]

a) Find the data hazards in the code segment. Indicate which instructions are causing what kind of hazard due to which register dependence.

b) Draw the busses in use for forwarding in each hazard using copies of the attached diagram [MIPS.jpg]. Label what is being forwarded.

c) Reorder the instructions to avoid any pipeline stalls.

d) Consider the new reordered sequence, draw a table to show where the instructions are in which stages in time for N cycles (pick N such that all the instructions complete). The table will have a column per pipeline stage (IF, ID, EX, MEM, WB) and a row per cycle. You can label the instructions i1 to i7 (but indicate which label corresponds to which instructions first).