Question 1) CMOS transistor level circuits

Part 1 (20 points): Draw the CMOS transistor level circuit that implements the following function: \( \neg((A + C)B) \). Use as few transistors as possible. Make sure to label ground, Vdd and the input and output signals. This problem will be graded on the quality of the circuit as well as its correctness.
Question 2) Flip-flops

Part 1 (15 points): Given the following flip-flop (PMOS transistors are not shown for simplicity):

Fill in the following table. If something cannot be known, place an X in that region.

<table>
<thead>
<tr>
<th>CLK</th>
<th>input</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Part 2 (5 points): Is this a positive edge triggered flip flop or negative edge triggered flip flop?
Question 3) Full Adders

Part 1 (10 points): Draw the gate-level circuit for a full adder. Clearly label the inputs, and outputs.

![Gate-level circuit for a full adder](image)

Part 2 (10 points): Implement a full adder using two 8:1 multiplexers. The inputs of the multiplexers can only be connected to Vdd, GND or the inputs of your full adder.

![Implementation of a full adder using 8:1 multiplexers](image)
Question 4) Arithmetic Circuits (2 pages!)

Part 1 (10 points): Design a circuit using only full adders (FA) and half adders (HA) that computes the sum of three unsigned 3-bit integers A[2:0], B[2:0], C[2:0]. You will be graded based on correctness and efficiency.

Your full adders and half adders can be represented as block diagrams. For each adder, indicate which output is the sum, and which output is the carry. Make sure to clearly label your circuit to leave no room for ambiguity.

HA: 2 inputs, 2 outputs
FA: 3 inputs, 2 outputs

HA: delay from input to C0: 1 x 2-input gate \therefore \text{delay}_{HA-C} = 3 \text{ FO1}
delay from input to S: 1 x 2-input gate \therefore \text{delay}_{HA-S} = 3 \text{ FO1}
FA: delay from input to S: 1 x 3-input gate \therefore \text{delay}_{FA-S} = 5 \text{ FO1}
delay from input to C0: 1 x 2-input gate + 1 x 3-input gate \therefore \text{delay}_{FA-C} = 8 \text{ FO1}

we assume the following adder:

\[ \begin{align*}
A &\rightarrow \text{ S} \\
B &\rightarrow \text{ Cin} \\
&\rightarrow \text{ C0}
\end{align*} \]

\[ \text{critical path delay is} \quad \text{delay}_{HA-C} + \text{delay}_{FA-S} + \text{delay}_{FA-C} + \text{delay}_{FA-C} + \text{delay}_{HA-C} \]

\[ = 3 + 5 + 8 + 3 = 27 \text{ FO1} \]
Part 2 (10 points):

Based on the following delays:
1 input gate = 1 FO1
2 input gate = 3 FO1
3 input gate = 5 FO1

(4 points) What is the critical path of your circuit (indicate on your diagram)?

(6 points) What is the critical path delay of your circuit? Show your work and state your assumptions.

\[
\text{Critical path delay is:} \\
\text{delay}_{FA-C} + \text{delay}_{FA-C} + \text{delay}_{HA-S} + \text{delay}_{FA-C} + \text{delay}_{HA-C} \\
= 2 + 2 + 5 + 2 + 2 \\
= 32 \text{ FO1} \\
\]

\[
\text{Answer then Soln 1} \\
\text{but 1 FO1 HA used!}
\]
Sdn 3

Critical path delay = delay FA - c + delay HA - c + delay FA - c + delay HA - c
= 8 + 3 + 8 + 3
= 22 F01

:. Faster than Sdn 1 & Sdn 2!

Same resources as Sdn 1
Question 5) Short answer (2 pages!)

4.1) (3 points) Order SRAM, DRAM and flip-flop by increasing number of transistors used per bit cell.

SRAM, DRAM, flip-flop

4.2) (3 points) Provide one reason for using FPGAs vs. ASIC to implement a product.

- Lower up-front cost
- Faster time to market
- Smaller design cycle
- Field reprogrammability

4.3) (3 points) Why are glitches undesirable?

Glitches consume power

4.4) (3 points) Discuss the area and delay trade-offs between using a ripple-carry adder vs. a carry-select adder:

Ripple carry adder: smaller area but longer delay
Carry select adder: larger area but shorter delay
4.5) (4 points) What does this circuit implement?

![A 2:1 MUX diagram]

4.6) (4 points) This is the LFSR that you put together in Lab 3:

Derives the values of A, B, C, D at every clock tick for 4 consecutive clock ticks.

<table>
<thead>
<tr>
<th>Time</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
</tr>
</thead>
<tbody>
<tr>
<td>t=0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>t=1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>t=2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>t=3</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>t=4</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>